1 General Description

The SC32F15G is a series of industrial-grade Flash microcontrollers based on the Arm Cortex®-M0+ core.

These microcontrollers operate at a high frequency of up to 72MHz. The Cortex®-M0+ core utilizes a 32-bit reduced instruction set architecture (RISC) and complies with the CMSIS standard. The SC32F15G series offers powerful data processing capabilities, with an integrated Direct Memory Access (DMA) controller for high-speed data transfer. The hardware CRC module and the built-in 32-bit hardware multiplier further enhance the data computation speed.

The SC32F15G microcontrollers incorporate two clock sources: a high-precision high-frequency 72MHz oscillator (HIRC), a low-frequency 32kHz oscillator (LIRC). Additionally, they provide a 32.768 kHz low-frequency crystal (LXT) interface. The embedded clock sources and external crystal oscillator interfaces can supply the system clock, and the built-in system clock monitor module switches to HIRC as the clock source in case of system clock abnormalities.

The SC32F15G series offers a wide range of peripheral resources, including up to 45 GPIO pins with external interrupt support, 4 16-bit timers, 3 independent UARTs, among which UART2 features a complete LIN interface and support both master and slave modes. 1 independent CAN interface (supporting CAN Specification 2.0B and CAN FD), 2 SPIs, 2 TWIs, 2 independent QEP modules, 3 analog comparator CMP0-2 sharing a common inverting input terminal and 1 independent analog comparator CMP3.It also features 3 independent rail-to-rail OP, 1 10-bit DAC, 18 channels of 12-bit high-precision ADC(supporting threshold alarm) and a temperature sensor module. The microcontrollers come with an independent watchdog timer (WDT) and a low-voltage reset circuit (LVR) to enhance system reliability. They provide three power modes to meet various power consumption requirements in different application scenarios.

The SC32F15G series supporting a wide operating voltage range of 2.0-5.5V and capable of operating in an ambient temperature range of -40°C to 105°C. They also exhibit excellent ESD performance and EFT immunity. In terms of process technology, the SC32F15G series adopts the industry-leading eFlash process, allowing for more than 100,000 write cycles and data retention of 100 years at room temperature. Regarding storage resources, the SC32F15G series offers a maximum of 128 Kbytes of ROM space and 8 Kbytes of SRAM The SRAM also supports parity check functionality for data integrity. Additionally, there is a 2 Kbytes user storage area(generic EEPROM), and a 4 Kbytes system storage area(LDROM). It includes a built-in system storage area to support OTA upgrades and provides multiple programming methods such as ISP (In-System Programming), ICP (In-Circuit Programming), and IAP (In-Application Programming), enabling on-board debugging and firmware updates while the chip is online or powered.

The SC32F15G series possesses outstanding anti-interference performance. It can be adapted to various master control solutions, finding applications in a wide range of industries including smart appliances, smart homes, the Internet of Things (IoT), new energy sector, industrial control, and consumer electronics.

2 Features

Operating Conditions

- Operating voltage: 2.0V to 5.5V
- Operating temperature: -40 to +105℃

EMS

- ESD
  - HBM：JS-001-2023 Class 3A
  - MM：JEDEC EIA/JESD22-A115 Class C
  - CDM：ANSI/ESDA/JEDEC JS-002-2022 Class C3
- EFT
  - EN61000-4-4 Level 4

Package

- 48 PIN: LQFP48 (7X7) / QFN48 (5X5)
- 32 PIN: LQFP32 (7X7) / QFN32 (4X4)
- 28 PIN: TSSOP28

Core

- Cortex®-M0+ core
- With Wakeup Interrupt Controller (WIC) module
- 64-bits instruction prefetch
- Built-in Multiplier Unit (MDU)

Reset

- Power-On Reset (POR)
- Software Reset
- Reset through external NRST pin (PC11) with a low-level signal
- Watchdog Timer (WDT) reset
- Low Voltage Reset (LVR)
  - Four selectable reset voltages: 4.3V, 3.7V, 2.9V, 1.9V
  - The default value is determined by the user's programmed Code Option

BUS

- 1 IOPORT
- 1 AHB
- 3 APB：APB0-APB2

Power Saving Mode

- Low-Speed Mode, system clock source can be selected as LIRC, and CPU can work at 32MHz
- IDLE Mode, can be woken up by any interrupt
- STOP Mode, can be woken up by INT0-15, Base Timer, TK, and CMP

2.1 Flash

APROM

- Up to 128 Kbytes APROM
- Can be rewritten up to 100,000 times
- Supports hardware read protection encryption
- Supports hardware write protection: Provides two regions for disabling IAP (In-Application Programming) operations. Users can configure the settings through the Code Option, with the minimum setting unit being 512 bytes (one sector)

LDROM

- 4 Kbytes of system storage area, factory-programmed with BootLoader program

SRAM

- 8 Kbytes Internal SRAM
- Supports parity check:
  - An additional 1K RAM is used for parity checking, which means SRAM data bus width is 36 bits, with 4 bits dedicated to parity check (one bit per byte).
  - The parity check bits are calculated and saved when writing to the SRAM, and automatically verified upon reading. If a bit fails, an unmaskable interrupt (Cortex®-M0+ NMI) will be generated.
  - Provides an independent SRAM parity error flag, SRAMPEIF.
  - Pay attention to the initialization of the SRAM when in use.
- Supports booting from SRAM

2K Bytes User Storage Area(generic EEPROM)

- Divided into four 512 bytes sectors
- Can be rewritten up to 100,000 times
- Data retention time is over 100 years at room temperature

96 Bits unique ID

- 96-bit Unique ID defined in the design option area

2.2 BootLoader

- Hardware method: System storage area of 4 Kbytes, factory-programmed with BootLoader program
- Software method: Supports interrupt vector table remapping, allowing flexible partitioning of the APROM area for user BootLoader program execution

2.3 Flash Programming and Emulation

- Programming methods supported: ICP / ISP / IAP
- 2-wire JTAG / SWD programming and emulation interface
- Simulation functionality is not supported in encrypted mode

2.4 Clock source

Built-in high-frequency 72 MHz oscillator (HIRC)

- Can be selected as the system clock source
- The default clock frequency when power on "f_{SYS}" is $f_{HIRC}/2$
- Frequency Error: Within ±1% @ -40 to 105℃ @ 2.0V to 5.5V
- The system clock can be automatically calibrated by 32.768 kHz external crystal oscillator, after calibration HIRC accuracy can be infinitely close to the accuracy of external 32.768 kHz crystal oscillator

Built-in low-frequency 32 kHz oscillator (LIRC)

- Can be selected as the system clock source
- Fixed as the WDT clock source, which will be automaticlly enabled when WDT is enabled
- Can be selected as the Base Timer clock source and can wake up from stop mode
- Frequency Error: Within ±4% @ -20 to 85℃ @ 4.0V to 5.5V, after register correction

External 32.768 kHz crystal oscillator (LXT)

- Can be selected as the system clock source
- Can be selected as the Base Timer clock source and can wake up from stop mode
- Allows for an external 32.768kHz oscillator
- Automatic calibration of HIRC can be performed using LXT

2.5 Interrupts (INT)

- Up to 25 interrupts
- Four-level interrupt priority can be set
- External interrupts (INT):
  - 16 interrupts, occupying 4 interrupt vectors in total
  - Change Interrupts on All GPIO pins
  - All interrupts can be set as rising edge, falling edge, or both-edge interrupts, each with an independent corresponding interrupt flag
  - Setting the corresponding interrupt flag in software triggers entry into the corresponding interrupt

2.6 Digtial peripherals

Up to 45 GPIOs

- Independent pull-up resistor configuration is available
- All GPIO pins have source driving capability controlled by four levels
- All GPIO pins have high sink current driving capability (50mA)

Watchdog timer (WDT)

- Built-in WDT with programmable overflow time ranging from 3.94ms to 500ms

Base Timer（BTM）

- The clock sources LXT and LIRC are selectable
- Selectable interrupt frequency intervals from 15.625ms to 32s
- Can wake up from STOP Mode

4 16-bit timers: Timer0-Timer3

- 16-bit up, down, and up/down auto-reload counters
- Supports rising edge/falling edge capture for PWM duty and period capture
- Each TIM can provide two channels of synchronized and adjustable duty cycle PWM outputs (TPWMA/TPWMB).
- TIM1/2 timer overflow and capture events can trigger DMA requests

2 independent quadrature encoder pulse (QEP) module

- Can be connected to linear or rotary incremental encoders to obtain machine position, direction, and speed information.
- Counting Modes:
  - Quadrature Counting
  - Direction Counting
  - Dual Pulse Counting
- Each QEP module (n = 0-1) provides three input signal pins: QEPnA, QEPnB and QEPnI
  - QEPnA and QEPnB can be swapped in direction
  - The polarity of QEPnA and QEPnB can be individually configured
  - Provides a configurable digital filter with a maximum division factor of 128 for QEPnA, QEPnB, and QEPnI signals
- In Direction Counting and Dual Pulse Counting modes, counting can be configured for:
  - Rising edge
  - Falling edge
  - Both edges (rising and falling)
- Position Counter Reset Modes:
  - Index Event Reset
  - overflow Reset
- Supports four interrupt sources:
  - Overflow Interrupt
  - Underflow Interrupt
  - Index Reset Interrupt
  - Edge Trigger Interrupt

3 independent UART: UART0-2

- UART2 has a full LIN interface, offering the following capabilities:
  - Master and slave mode switching
  - Hardware break transmission in master mode(10/13bits)
  - Hardware break detection in slave mode(10/11bits)
  - Baud rate synchronization in slave mode
  - Provision of related interrupts, status bits, and flags
- Each UART ports can be mapped to 2 sets of IO pins
- Independent baud rate generator
- UART2 does not support wake-up from STOP Mode
- UART0/1 support wake-up from STOP Mode
- Three communication modes available
  - Mode 0: 8-bit half-duplex synchronous communication
  - Mode 1: 10-bit full-duplex asynchronous communication
  - Mode 3: 11-bit full-duplex asynchronous communication
- UART0 and UART1 support DMA requests
- UART2 do not support DMA requests

1 independent SPI: SPI0

- SPI0:
  - A 16-bit 8-level FIFO with separate transmit and receive
  - In SPI mode, the drive capability of the corresponding signal pins will be enhanced
  - Can be mapped to 2 sets of ports
  - Supports DMA

1 independent TWI: TWI0

- Supports master mode or slave mode
- Supports clock stretching in slave mode
- Communication speed of up to 1Mbps
- TWI0 supports DMA
- TWI0 signal ports can be mapped to 3 set of ports

1 dual-function interface SP1&TWI1

- SPI1 and TWI1 operate independently with multiplexed register addresses and signal pins
- SPI1 and TWI1 can be mapped to 4 sets of ports
- SPI1 supports DMA
- TWI1
  - Supports master mode or slave mode
  - Supports clock stretching in slave mode
  - Communication speed of up to 1Mbps

CAN

- Protocol Support:
  - CAN 2.0B
  - CAN FD
- Supports low-power standby mode to reduce power consumption when the CAN interface is idle
- Time-Stamping:
  - CiA 603 Compliance, provides a 64-bit time-stamp for precise timing, each transmitted frame has one time-stamp stored in a register, and all received frames have individual time-stamps
- Transmit and Receive Buffers:
  - 8 Receive Buffers (RB)
  - 9 Transmit Buffers (TB)
    - PTB(Primary Transmission Buffer)
    - STB(Secondary Transmission Buffer)
  - 8 Receive Filters: Support 29-bit identifiers for filtering incoming messages

CRC

- Initial value can be set, with a default of 0xFFFF_FFFF
- Polynomial can be programmed, with a default of 0x04C1_1DB7
- Supports 8/16/32-bit data units

DMA

- 4 independent configurable channels
- Each DMA channel can send DMA requests to other channels
- Data width supports byte, half-word, and word
- 21 DMA request sources with four priority levels
- Supports source/destination address auto-increment or fixed
- Supports single and burst transfer modes
- Transfer modes: memory to memory, memory to peripheral, peripheral to memory, peripheral to peripheral

2.7 Analog peripherals

5 reference voltage for analog peripherals

- VDD
- 2.4V
- 2.048V
- 1.024V
- External Vref PIN input source

Internal reference source VREF

- 3 built-in reference voltage:2.4V,2.048V and 1.024V
- External Vref PIN input source is optional source for analog peripherals
- VDD is optional source for analog peripherals
- Each ADC / DAC / OP can independently select reference source is from VREF or VDD

Digital-to-Analog Converter DAC

- Precison: 10 bits
- Output ports:
  - 2 independent DAC output port DACOUT0 and DACOUT1
  - Inverting input port of OP1/OP2
  - Negative port of CMP0/1/2/3

Analog-to-Digital Converter ADC

- Precison: 12 bits
- Supports up to 18 channels
  - External 16 ADC sampling channels can be multiplexed with I/O ports for other functions
  - Output port of OP0,OP1,OP2 are multiplexed with ADC channels, and the output value can be directly read through ADCV register
  - One internal ADC can directly measure VDD voltage
  - One internal temperature sample channel
- Configurable ADC upper and lower threshold, which can trigger interrupt
- Selectable trigger mode:
  - Manual Trigger
  - Sequential Trigger(Only available through software trigger)
- Configurable ADC conversion completion interrupt
- Single-channel conversion time:404ns
- Supports DMA transmission: DMA request will be generated after ADC conversion complete
- The conversion results feature an overflow flag: OVERRUN, and the OVERRUN flag bit is located in the same register as the ADC conversion results so users can read the information all at once.

Operational Amplifier(OP)

- 3 independent rail-to-rail operational amplifiers:OP0/OP1/OP2
- OP1/OP2 can be configurable as CMP
  - Comparator voltage hysteresis: 10-15mV
  - Response time: typical 50ns
- All three OPs can be configurable as a Programmable Gain Amplifier (PGA)
  - Non-inverting gain: 4/8/16/32
  - Inverting gain: 3/7/15/31
- All three OPs have independent non-inverting input port, inverting input port and output port
- Output port of OP0,OP1,OP2 are multiplexed with ADC channels, and the output value can be directly read through ADCV register
- The output of OP1/OP2 can be directly connected to the positive input of CMP0 and CMP3
- Offset voltage≤10mV, and need zero calibration
- Slew rate≥10V/us

3 Analog Comparator CMP0/1/2

- CMP0/1/2 have indenpendent external input port
- Positive input of CMP0 can select the output of OP1 and OP2
- Negative input of CMP0/1/2 selectable:
  - Shared input port CMPxN
  - Internal DAC output
- CMP0/1/2 interrupts can wake up the STOP mode
- Comparator voltage hysteresis: 0/5/10/20mV
- Response time: typical 50ns

1 Independent Comparator CMP3

- Positive input of CMP3 selectable:
  - External input port CMP3N
  - Internal OP1 or OP2 output
- Negative input of CMP3 selectable:
  - External input port CMP3N
  - Internal DAC output
  - 16-level Vref voltage divider module output
- CMP3 interrupts can wake up the STOP mode
- Comparator voltage hysteresis: 0/5/10/20mV
- Response time: typical 50ns

Temperature Sensor

- The volatege value of temperature sensor can be measured by ADC
  - Use internal 2.4V as reference voltage
  - The conversion value of ADC will increase by a fixed value for every increase of 1℃

Product Peripheral Resourse Table

Model Peripherals	SC32F15G					
	_C7	_K7	_G7	_C6	_K6	_G6
GPIOs	45	30	26	45	30	26
APROM (Kbyte)	128			64		
SRAM (Kbyte)	8					
SPI	2					
TWI	2					
UART	3					
TIM	4					
OP	3	2		3	2	
CMP	4	3		4	3	
DAC Channels	1					
ADC Channels	18	15	13	18	15	13
QEP	2	1	0	2	1	0
CAN	1		-	1		-
CRC	YES					
DMA	YES					
Temperature Sensor	YES					
Max. CPU frequency	72MHz					

Products naming rules

SC 32 F 1 5 G C 7 P J R

Campany Name
SinOne

Device famliy
8=8bit
32=32bit

Device thpe
A=Automotive
F/G=General
L=Ultra-low power
H=High performance
W=Wireless
M=Motor

CPU core
0= Cortex-M0
1= Cortex-M0+

Subseries1
0~9

Subseries2
T=TK
G=GP
M=Motor

Pin count

Label	D	F	E	G	K	T	H	S	C	U	R	J	M	O
Pin count	14	20	24	28	32	36	40	44	48	63	64	72	80	90
Label	V	Q	Z	A	I	B	N	X						
Pin count	100	132	144	169	176	208	216	256						

Flash memory size

Label	0	1	2	3	4	5	6	7	8	9	A	B	C	D
Size(KB)	1	2	4	8	16	32	64	128	256	512	1024	2048	-	-
Label	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Size(KB)	-	-	-	-	-	-	-	72	96	192	384	768	1536	-

Package type

Label	D	M	X	F	T	P	Q	K	S	Y	H	U	W
Package	DIP	SOP	TSSOP	QFP	TQFP	LQFP	QFN	SKDIP	MSOP	WLCSP	BGA	SOT	Wafer

Temperature range
I= -40°C~85°C Industrial
J= -40°C~105°C Automotive G2
A= -40°C~125°C Automotive G1
T= -40°C~150°C Automotive G0

Pack type

R	Tray
T	Tape and Reel
U	Tube
B	Bulk

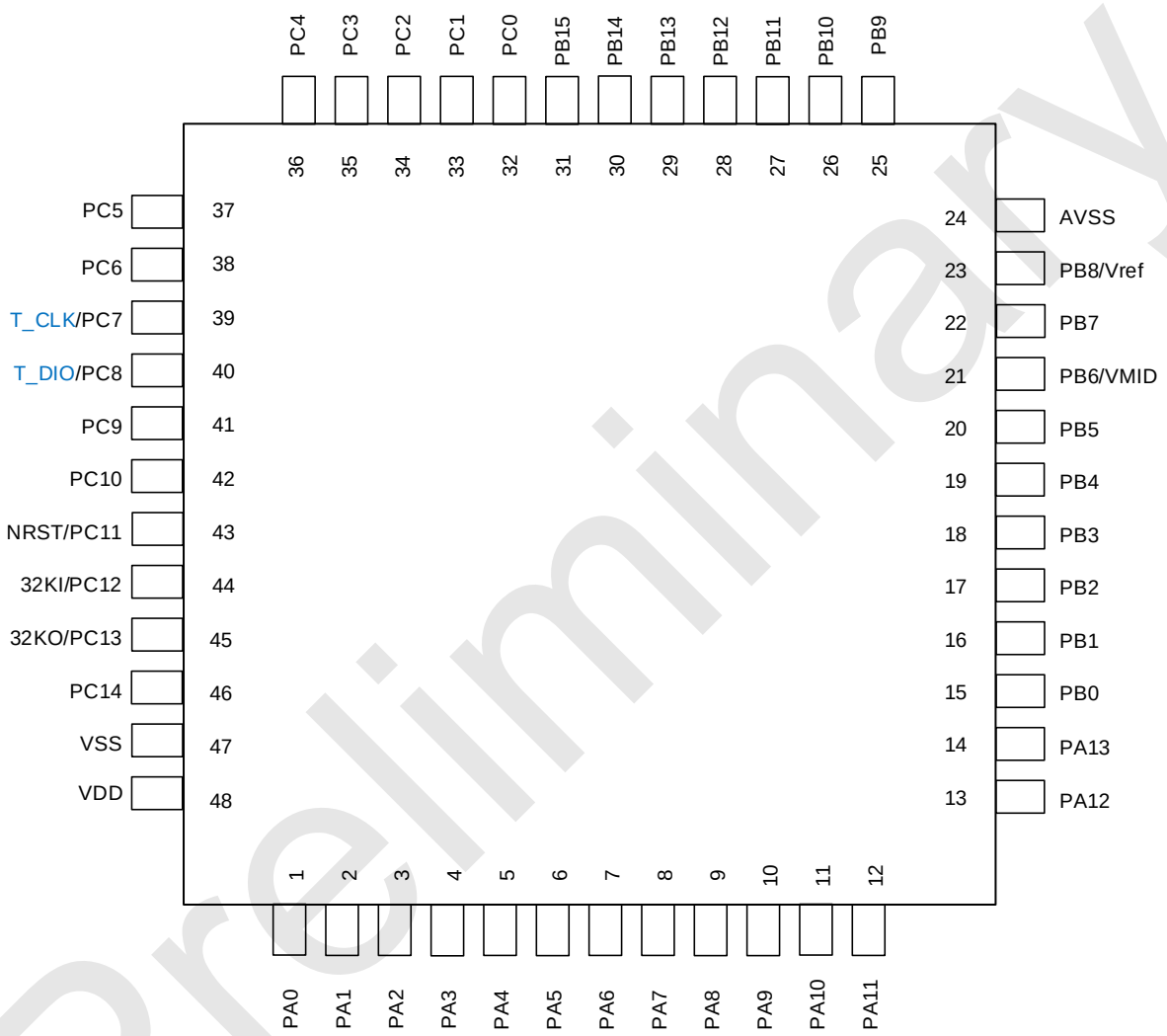
Ordering Information

PRODUCT ID	PACKAGE	PACK
SC32F15GC7PJR	LQFP48	Tray
SC32F15GC6PJR	LQFP48	Tray
SC32F15GC7QJR	QFN48	Tray
SC32F15GC6QJR	QFN48	Tray
SC32F15GK7PJR	LQFP32	Tray
SC32F15GK6PJR	LQFP32	Tray
SC32F15GK7QJR	QFN32	Tray
SC32F15GK6QJR	QFN32	Tray
SC32F15GG7XJU	TSSOP28	Tube
SC32F15GG6XJU	TSSOP28	Tube

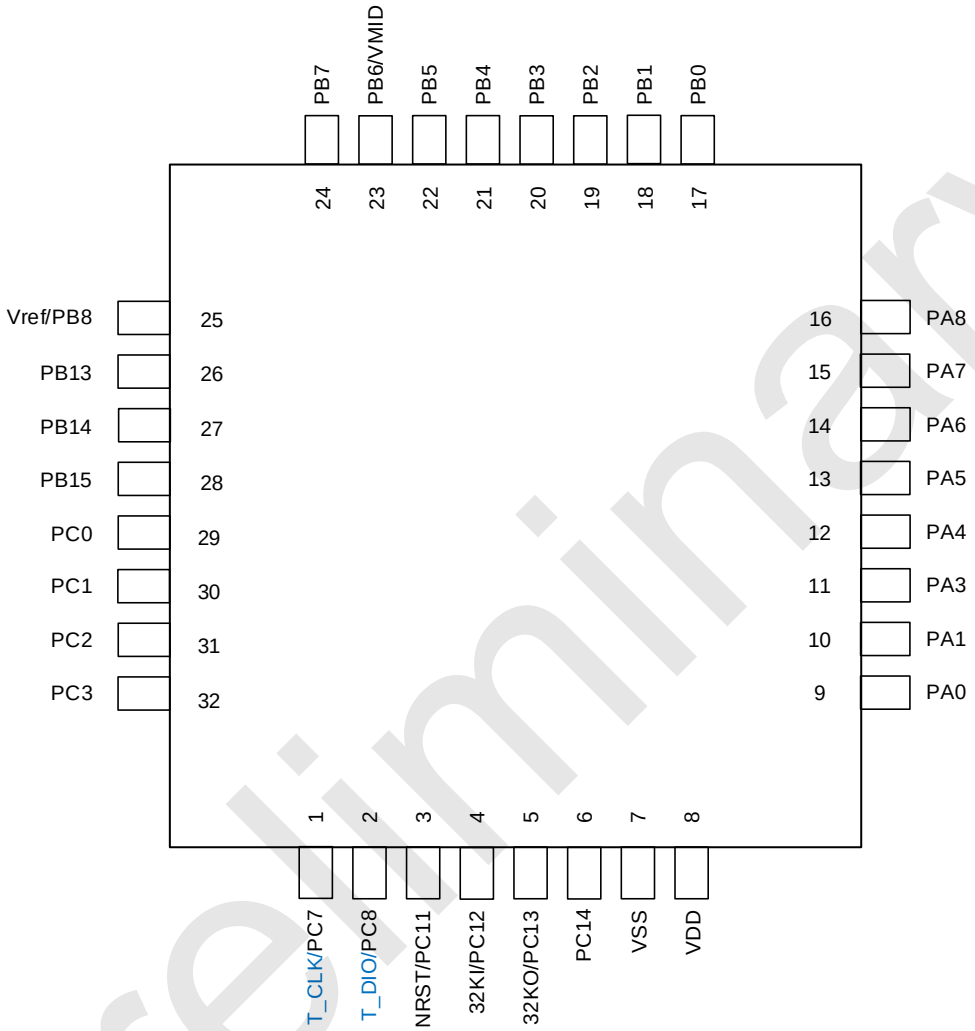
Content

3 Pin Description

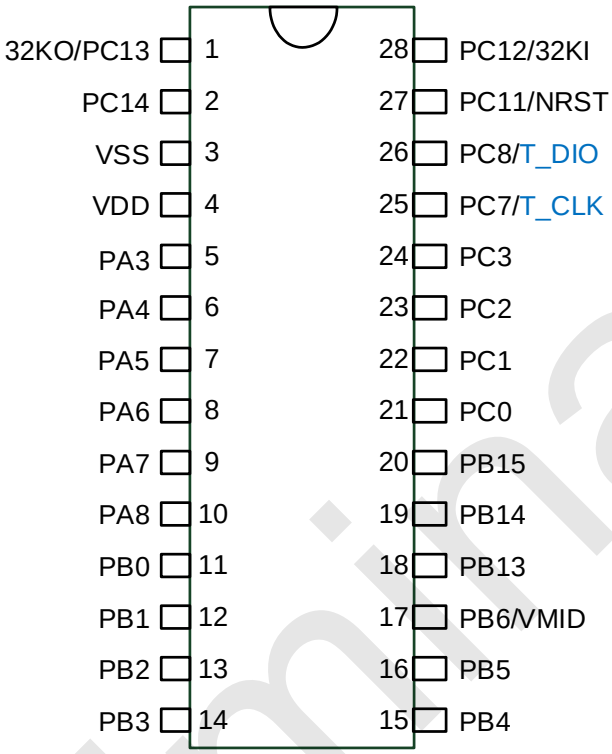
3.1 Pin Configuration



48PIN Pin Diagram
Suitable for LQFP48 & QFN48 package



32PIN Pin Diagram
Suitable for LQFP32 & QFN32 package



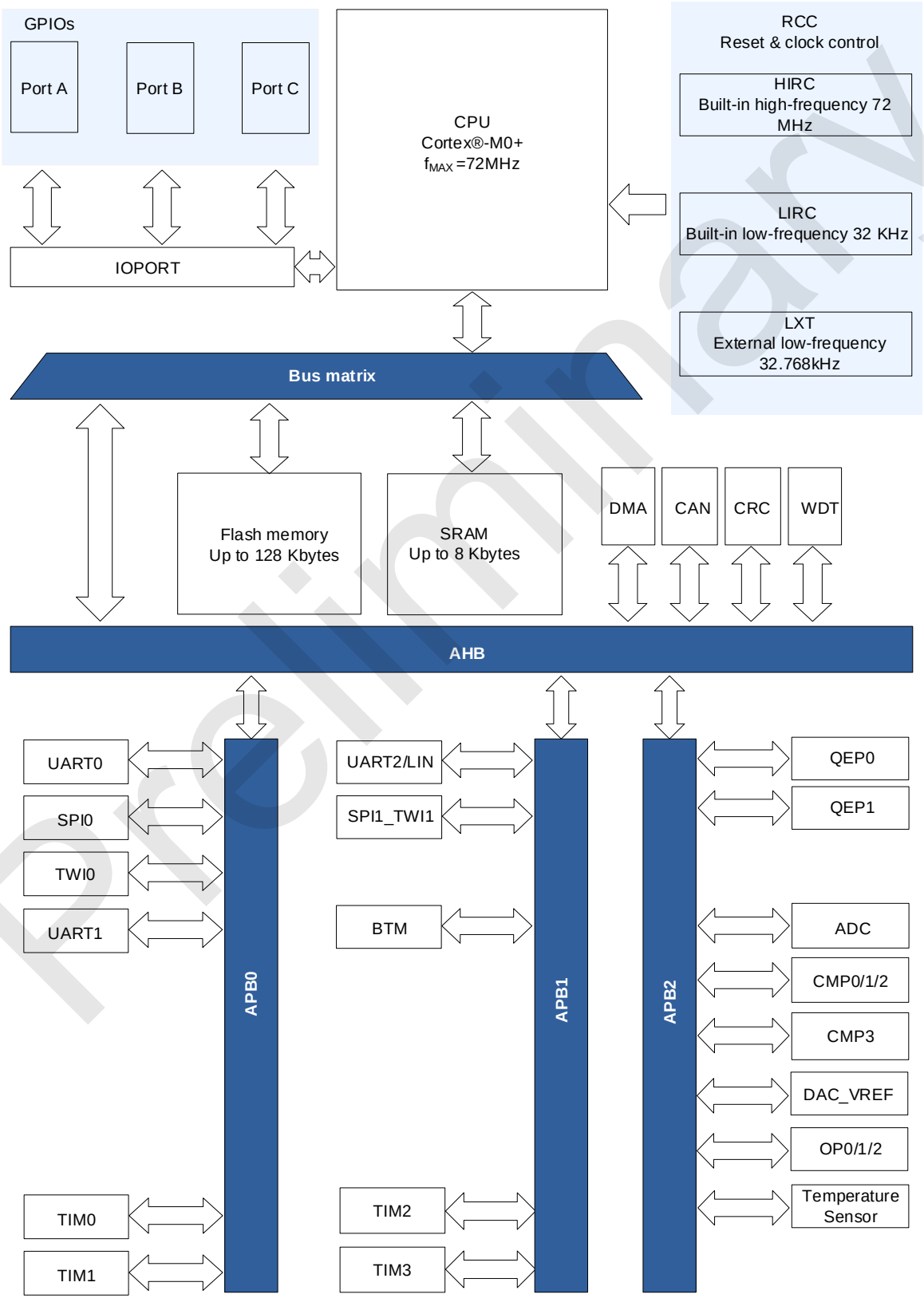
28PIN Pin Diagram
Suitable for TSSOP28 package

3.2 Pin Resource List

LQFP48/QFN48	LQFP32/QFN32	TSSOP28	Pin Name	Special	OP	CMP	DAC	ADC	QEP	TPWM	TIM	UART	SPI	TWI	CAN	INT
1	9	-	PA0	-	-	-	-	-	QEP1A	-	-	TX2(LIN)	-	SCL0	-	INT00
2	10	-	PA1	-	-	-	-	-	QEP1B	-	-	RX2(LIN)	-	SDA0	-	INT01
3	-	-	PA2	-	-	-	-	-	QEP1I	-	-	-	-	-	-	INT02
4	11	5	PA3	-	-	-	-	-	-	-	-	-	-	-	-	INT03
5	12	6	PA4	-	-	-	-	-	-	T0PWMA	T0CAP/T0	-	-	-	-	INT04
6	13	7	PA5	-	-	-	-	-	-	T0PWMB	T0EX	-	-	-	-	INT05
7	14	8	PA6	-	-	-	-	-	-	-	-	-	SCK1A	SCL1A	-	INT06
8	15	9	PA7	-	-	-	-	-	-	-	-	-	MOSI1A	SDA1A	-	INT07
9	16	10	PA8	-	-	-	-	-	-	-	-	-	MISO1A	-	-	INT08
10	-	-	PA9	-	-	-	-	-	-	-	-	-	-	-	-	INT09
11	-	-	PA10	-	-	-	-	-	-	-	-	-	-	-	-	INT10
12	-	-	PA11	-	-	-	-	-	-	-	-	-	SCK1B	SCL1B	-	INT11
13	-	-	PA12	-	-	-	-	-	-	-	-	-	MOSI1B	SDA1B	-	INT12
14	-	-	PA13	-	-	-	-	-	-	-	-	-	MISO1B	-	-	INT13
15	17	11	PB0	-	OP0P	-	-	-	-	(T0PWMA)	(T0CAP/T0)	TX2A	-	-	-	INT00
16	18	12	PB1	-	OP0N	-	-	-	-	(T0PWMB)	(T0EX)	RX2A	-	-	-	INT01
17	19	13	PB2	-	OP0O	-	-	AIN0	-	(T1PWMA)	(T1CAP/T1)	-	SCK1C	SCL1C	-	INT02
18	20	14	PB3	-	OP1P	-	-	-	-	(T1PWMB)	(T1EX)	RX1A	MOSI1C	SDA1C/SCL0B	-	INT03
19	21	15	PB4	-	OP1N	-	-	-	-	(T2PWMA)	(T2CAP/T2)	TX1A	MISO1C	SDA0B	-	INT04
20	22	16	PB5	-	OP1O	-	-	AIN1	-	(T2PWMB)	(T2EX)	TX0A	MISO0A	-	-	INT05
21	23	17	PB6	VMID	-	-	-	AIN2	-	(T3PWMA)	(T3CAP/T3)	RX0A	MOSI0A	SDA0A	-	INT06
22	24	-	PB7	-	-	-	DACOUT0	AIN3	-	(T3PWMB)	(T3EX)	-	SCK0A	SCL0A	-	INT07
23	25	-	PB8	Vref	-	-	-	AIN4	-	-	-	-	-	-	-	INT08
24	-	-	AVSS	-	-	-	-	-	-	-	-	-	-	-	-	-
25	-	-	PB9	-	-	-	-	AIN5	-	-	-	-	-	-	-	INT09
26	-	-	PB10	-	OP2P	-	-	-	-	-	-	-	-	-	-	INT10

LQFP48/QFN48	LQFP32/QFN32	TSSOP28	Pin Name	Special	OP	CMP	DAC	ADC	QEP	TPWM	TIM	UART	SPI	TWI	CAN	INT
27	-	-	PB11	-	OP2N	-	-	-	-	-	-	-	-	-	-	INT11
28	-	-	PB12	-	OP2O	-	-	AIN6	-	-	-	-	-	-	-	INT12
29	26	18	PB13	-	-	CMPxN	-	AIN7	-	-	-	-	-	-	-	INT13
30	27	19	PB14	-	-	CMP0P	-	AIN8	-	-	-	-	SCK1	SCL1	-	INT14
31	28	20	PB15	-	-	CMP1P	-	AIN9	-	-	-	-	MOSI1	SDA1	-	INT15
32	29	21	PC0	-	-	CMP2P	-	AIN10	-	-	-	-	MISO1	-	-	INT00
33	30	22	PC1	-	-	-	-	AIN11	-	T3PWMB	T3EX	RX1	MISO0	-	CAN_RX	INT01
34	31	23	PC2	-	-	-	-	AIN12	-	T3PWMA	T3CAP/T3	TX1	MOSI0	-	CAN_TX	INT02
35	32	24	PC3	-	-	-	-	AIN13	-	-	-	-	SCK0	-	-	INT03
36	-	-	PC4	-	-	CMP3N	-	-	（QEP1A）	-	-	-	-	-	-	INT04
37	-	-	PC5	-	-	CMP3P	-	-	（QEP1B）	-	-	-	-	-	-	INT05
38	-	-	PC6	-	-	-	DACOUT1	AIN14	（QEP1I）	(T0PWMA)	(T0CAP/T0)	-	-	-	-	INT06
39	1	25	PC7	T_CLK	-	-	-	-	-	(T0PWMB)	(T0EX)	RX0	-	-	-	INT07
40	2	26	PC8	T_DIO	-	-	-	-	-	-	-	TX0	-	-	-	INT08
41	-	-	PC9	-	-	-	-	-	QEP0A	-	-	-	-	-	-	INT09
42	-	-	PC10	-	-	-	-	-	QEP0B	-	-	-	-	-	-	INT10
43	3	27	PC11	NRST	-	-	-	-	QEP0I	T1PWMA	T1CAP/T1	-	-	-	-	INT11
44	4	28	PC12	32KI	-	-	-	-	-	T1PWMB	T1EX	-	-	-	-	INT12
45	5	1	PC13	32KO	-	-	-	-	-	T2PWMB	T2EX	-	-	-	-	INT13
46	6	2	PC14	-	-	-	-	AIN15	-	T2PWMA	T2CAP/T2	-	-	-	-	INT14
47	7	3	VSS	VSS	-	-	-	-	-	-	-	-	-	-	-	-
48	8	4	VDD	VDD	-	-	-	-	-	-	-	-	-	-	-	-

4 Resource Diagram

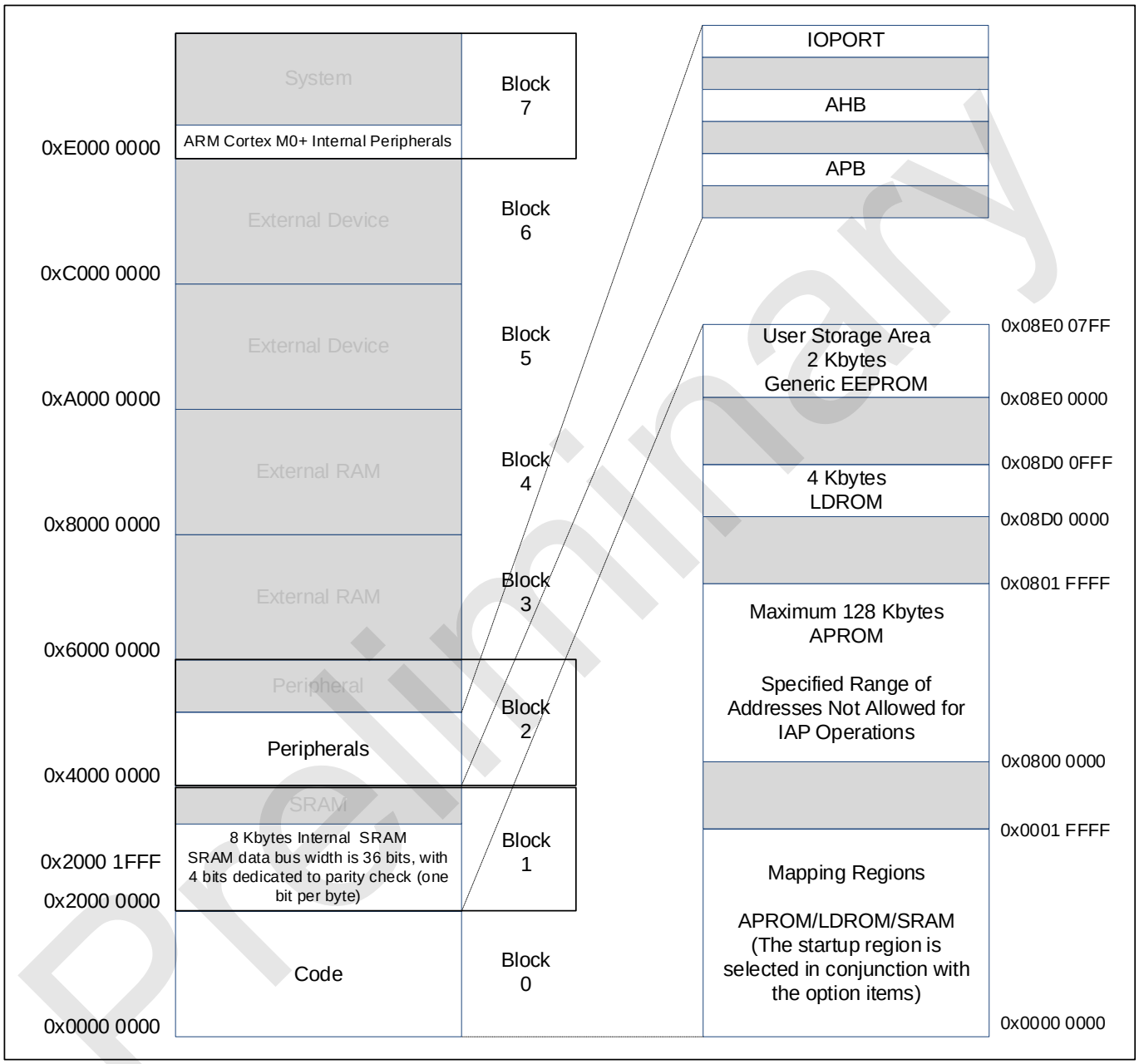


5 Flash

5.1 Overview

The program memory, data memory, and registers are arranged within a single linear (i.e., contiguous) 4 GB address space. Each byte is encoded in the storage in little-endian format, meaning that the least significant byte of a word is considered to be the lowest numbered byte, while the most significant byte is considered to be the highest numbered byte. The addressable storage space is divided into 8 main blocks, each block being 512 MB in size.

5.2 Storage Block Diagram



SC32F15G Series Memory Mapping Diagram

5.3 Feature

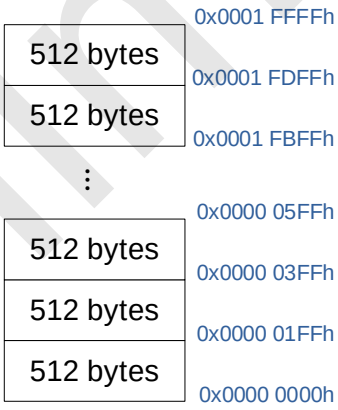
- The Flash width is 32 bits, and it can be rewritten up to 100,000 times
- Data retention time is over 100 years at room temperature
- The structure of the Flash includes:
  - Maximum 128 Kbytes APROM
  - 4 Kbytes LDROM

- 2 Kbytes user storage area (generic EEPROM)
- 8 Kbytes Internal SRAM, support parity check
- 96 bits Unique ID

5.4 APROM

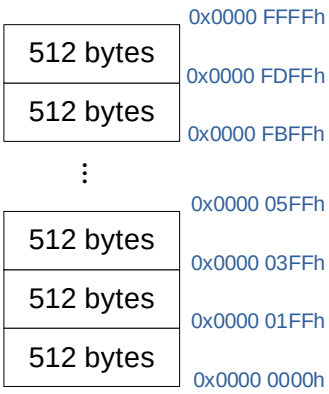
- Maximum 128 Kbytes APROM
- Sector Size: 512 bytes
- Supports: Read/Write/Sector Erase/Chip Erase/Blank Check
- The CPU (Cortex®-M0+) accesses Flash through the AHB bus
- The program defaults to booting from APROM, and users can select programs to boot from other areas such as SRAM/LDROM using the customer option OP_BL[1:0].
- Read Protection: After enabling read protection, only a program that runs from APROM can read information from APROM. Other areas or third-party tools cannot access information from APROM.
- Write Protection: Provides two hardware write protection regions where IAP operations are prohibited. Users can set the range of the two write protection regions in units of sectors based on actual needs.

128 Kbytes of APROM is divided into 256 sectors, with each sector being 512 bytes. During programming, the sector corresponding to the target address is forcibly erased by the programmer before writing data. For user write operations, erasure must precede data writing.



SC32F15G series 128 Kbytes APROM Sector Partition Illustration

64 Kbytes of APROM is divided into 128 sectors, with each sector being 512 bytes. During programming, the sector corresponding to the target address is forcibly erased by the programmer before writing data. For user write operations, erasure must precede data writing.

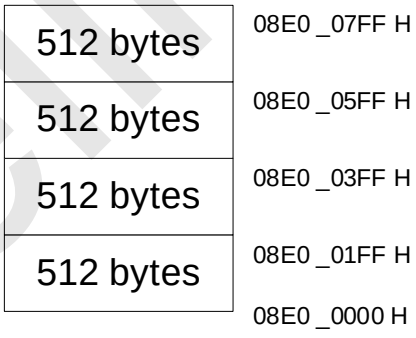


SC32F15G series 64 Kbytes APROM Sector Partition Illustration

5.5 2 Kbytes User Storage Area (Genetic EEPROM)

The 2 Kbytes of independent EEPROM area is addressed from 0x08E0_0000 H to 0x08E0_07FF H, as set by the IAPADE register. This independent EEPROM can be written to repeatedly up to 100,000 times, and it is designed to retain data for over 100 years at room temperature. The independent EEPROM supports various operations including blank check, programming, verification, erasure, and reading functions.

EEPROM has 4 sectors, with each sector being 512 bytes.



EEPROM Sector Partition Illustration

Note: The EEPROM has a write cycle endurance of 100,000 times. Users should avoid exceeding the rated write cycles of the EEPROM to prevent any anomalies!

5.6 4 Kbytes LDROM

- 4 Kbytes of system storage area, factory-programmed with BootLoader program, Users cannot modify or access this area.
- Embedded Bootloader Program: The fixed ISP program is publicly available, allowing reprogramming of Flash via UART. The program waits for upgrade commands, and if no update command is received within 500 milliseconds, it jumps to APROM for execution (0X0800 0000).

5.6.1 BootLoader

Supports two Bootloader modes:

- Software Approach: Directly partition BootLoader and APP areas in software. Easy sharing interrupts of BootLoader and APP by modifying VTOR. Flexible adjustment of the size of each area；
- Hardware Approach: 4 Kbytes fixed "LDROM" as a dedicated BootLoader area that users cannot read or write
  - LDROM serves as a fixed BootLoader space with factory-programmed program, and users cannot read or write
  - Embedded Bootloader Program: The embedded bootloader program resides in LDROM and is programmed during the production stage. The fixed ISP program is publicly available, allowing reprogramming of Flash via UART.

5.7 SRAM

- Internal SRAM：8 Kbytes，address 0x2000 0000 - 0x2000 1FFF
- Supports parity check
  - An additional 1K RAM is used for parity checking, which means SRAM data bus width is 36 bits, with 4 bits dedicated to parity check (one bit per byte).
  - The parity check bits are calculated and saved when writing to the SRAM, and automatically verified upon reading. If a bit fails, an unmaskable interrupt (Cortex®-M0+ NMI) will be generated.
  - Provides an independent SRAM parity error flag, SRAMPEIF.

Note: When SRAM parity check is enabled, it is recommended to perform a software initialization of the entire SRAM at the beginning of the code to prevent parity check errors when reading from uninitialized locations.

- Users can choose to start the program from SRAM by configuring the customer option OP_BL[1:0].
- It supports byte, half-word (16-bit), or word (32-bit) access at the maximum system clock frequency, with no waiting states. Therefore, it can be accessed by both the CPU and DMA

5.8 Boot Area Selection (Bootstrap)

After a reset, users can independently configure the desired bootstrap mode.

After exiting the standby mode, the startup mode configuration can be resampled. Once this startup delay has ended, the CPU will fetch the stack top value from address 0x00000000 and then begin executing code from the bootstrap memory starting at 0x00000004.

There are three options for bootstrap area selection: Main Flash Memory Area, System Flash Memory Area and SRAM, described in detail as follows:

5.8.1 Bootstrap from APROM

APROM is aliased in the bootstrap memory space (0x00000000) but can also be accessed from its original memory space (0x08000000). In other words, the program can start accessing from either address 0x00000000 or 0x08000000.

5.8.2 Bootstrap from LDROM

- 4 Kbytes LDROM serves as a fixed BootLoader space with factory-programmed program, Users cannot modify or access this area.
- Embedded Bootloader Program: The embedded bootloader program resides in LDROM and is programmed during the production stage. The fixed ISP program is publicly available, allowing reprogramming of Flash via UART.

5.8.3 Bootstrap from SRAM

SRAM has an alias in the bootstrap memory space (0x0000 0000) but can also be accessed from its original memory space (0x2000 0000).

5.8.4 Bootstrap mode config

The bootstrap modes can be controlled by the register bits BTLD[1:0] in conjunction with the software reset (RST) control bit, both protected by the IAP_KEY:：

① Set BTLD[1:0]=0x00: the chip boots from APROM after a software reset
② Set BTLD[1:0]=0x01: the chip boots from LDROM after a software reset
③ Set BTLD[1:0]=0x10: the chip boots from SRAM after a software reset

The initial boot region selection during power-up can be configured by customer option bits OP_BL[1:0]:

① Set OP_BL[1:0]=0x00 in customer option: the chip boots from APROM after a software reset
② Set OP_BL[1:0]=0x01 in customer option: the chip boots from LDROM after a software reset
③ Set OP_BL[1:0]=0x10 in customer option: the chip boots from SRAM after a software reset

5.9 96 bits Unique ID

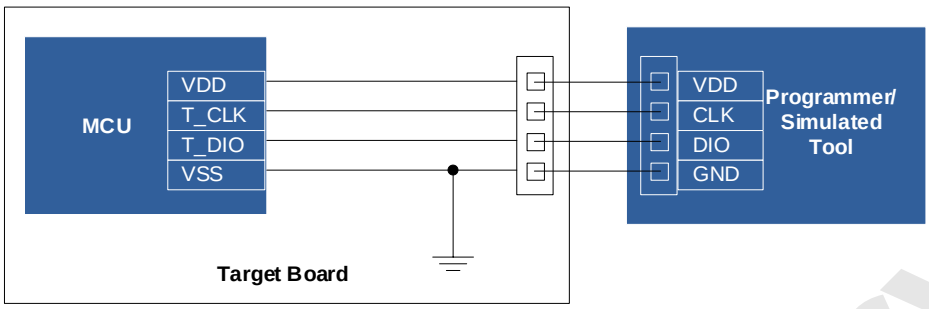
The SC32F15G provides an independent Unique ID area. A 96-bit unique code can be pre-programmed before leaving the factory to ensure the uniqueness of the chip. The only way for the user to obtain the serial number is to read through the IAP instruction.

5.10 User ID Area

User ID area, where user-costomized ID is pre-programmed when leaving the factory. Users can read the User ID area, but cannot write the User ID area.

5.11 Programming

The SC32F15G's Flash can be programmed through T_DIO, T_CLK, VDD, VSS, the specific connection relationship is as follows:



ICP mode Flash Writer programming connection diagram

T_DIO、T_CLK is a 2-wire JTAG programming and emulation signal line. Users can configure the mode of these two ports through the Customer Option when programming.

5.11.1 JTAG Specific Mode

T_DIO,T_CLK are specific port for programming and emulation, and other functions multiplexed with it are not available. This mode is generally used in the online debugging stage, which is convenient for users to simulate and debug. After the JTAG special mode takes effect, the chip can directly enter the programming or emulation mode without powering on and off again.

5.11.2 Normal Mode (JTAG specific port is invalid)

The JTAG function is not available, and other functions multiplexed with it can be used normally. This mode can prevent the programming port from occupying the MCU pins, which is convenient for users to maximize the use of MCU resources.

Note: When the invalid configuration setting of the JTAG dedicated port is successful, the chip must be completely powered off and then on again to enter the programming or emulation mode, which will affect the programming and emulation in the live mode. SinOne recommends that users select the invalid configuration of the JTAG dedicated port during mass production and programming, and select the JTAG mode during the development and debugging phase.

Related Customer Option is as followed:

Register	R/W	Description	Reset Value
COPT1_CFG@0xC2	R/W	Customer Option Mapping Register 1	0x0000_0000

7	6	5	4	3	2	1	0
ENWDT	DISJTG	DISRST	-	-	-	OP_BL[1:0]	

Bit number	Bit Mnemonic	Description
6	DISJTG	JTAG Ports Switch Control Bit

Bit number	Bit Mnemonic	Description
		0: JTAG mode enabled, the corresponding pins can only be used as T_CLK and T_DIO 1: Normal mode, JTAG function disabled

5.12 Security Encryption

- The SC32F15G series mainly involves encrypting the APROM for read protection. Users can configure the read protection encryption feature during programming through the customer option in the dedicated programming host; enable flash read protection can enter encryption mode: The chip defaults to a non-encrypted state while leaving the factory
- The read protection encryption feature has no mapped registers. Users can only modify it after config the customer option in the dedicated programming host and programming.
- Encryption Disabled: Operations such as reading, programming, and erasing can be performed on APROM. These operations can be also performed on Bytes and backup registers.
- Encryption Enabled:
  - Enable from APROM: Code executed in user mode (booting from user APROM) can perform all operations on APROM.
  - Debug, enable from SRAM and LDROM: In debug mode or when code is booted from SRAM or LDROM, APROM is completely inaccessible.
- Disabling encryption requires a full erase operation on APROM.

5.12.1 Security Encryption Access Rights

Boot Area/Tools	Encryption Disabled Status					Read Protection Encryption Status				
	Read	Write	Block Earse	Full Earse	Operate Write-Protection Region	Read	Write	Block Earse	Full Earse	Operate Write-Protection Region
Bootstrap from APROM	√	√	√	\	Forbid	√	√	√	\	Forbid
Debug/Bootstrap from SRAM	√	√	√	√	Forbid	Forbid	Forbid	Forbid	Forbid	Forbid
Bootstrap from LDROM	√	√	√	√	√	Forbid	Forbid	Forbid	√	Forbid

5.13 In Application Programming (IAP)

The IAP (In Application Programming) area in the APROM of SC32F15G allows users to perform remote program updates through IAP operations. Users can also retrieve information from the Unique ID or User ID areas by IAP read operations. Before performing IAP write operations, users must carry out sector erasure for the target address sector.

The chip allows global IAP operations in the APROM by default while leaving the factory. Internally, the chip provides two sets of APROM write protection regions. These regions are set based on sector units, and the

protected areas are restricted from IAP operations. The rules for setting these regions are as follows:

IAPPORx Register Value（x=A or B）	IAPPOR Protection Area
IAPPORx_ST = IAPPORx_ED	Sector IAPPORx
IAPPORx_ST > IAPPORx_ED	No protection
IAPPORx_ST < IAPPORx_ED	Sectors from IAPPORx_ST to IAPPORx_ED

User can config these APROM's write protection area through "Flash sectors protection" in Customer Option

6 Power,Reset And System Clock（RCC）

6.1 Power-on Reset

After the SC32F15G power-on, the processes carried out before execution of client software are as follows:

① Reset stage
② Loading information stage
③ Normal operation stage

6.1.1 Reset Stage

The SC32F15G will always be reset until the voltage supplied to SC32F15G is higher than a certain voltage, and the internal Clock starts to be effective. The duration of reset stage is related to rising speed of external power. Once the external supply voltage is up to built-in POR voltage, the reset stage would be completed.

6.1.2 Loading Information Stage

There is a warm-up counter inside The SC32F15G. During the reset stage, the warm-up counter is cleared to 0 until the voltage exceeds the POR voltage, the built-in HIRC oscillator starts to oscillate, and the warm-up counter starts counting. When the internal warm-up counter counts to a certain number, every certain number of HIRC clocks will read a byte of data from the IFB (including Customer Option) in the Flash ROM and store it in the internal system register. This reset signal will not end until the warm-up is completed.

6.1.3 Normal Operation Stage

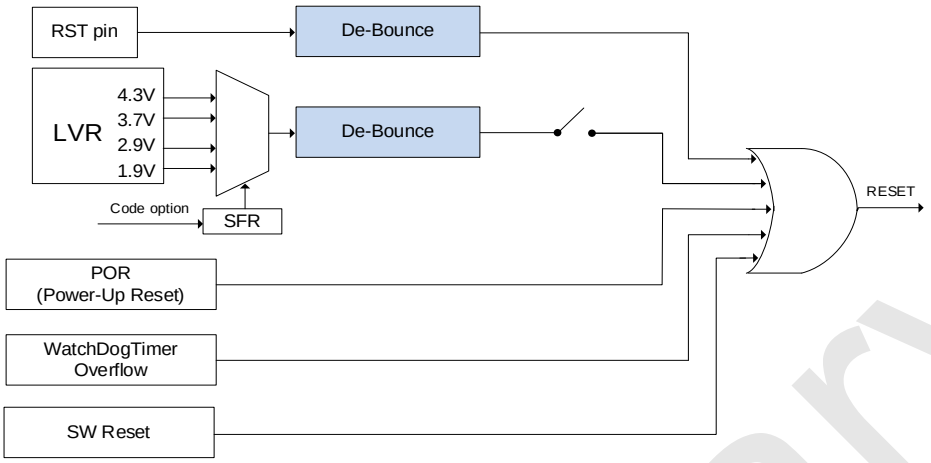
After finishing the Loading Information stage, The SC32F15G starts to read the instruction code from Flash and enters the normal operation stage. The LVR voltage is the set value of Customer Option written by the user.

6.2 Reset Modes

The SC32F15G has 5 reset methods, the first four are hardware reset:

- External reset
- Low-voltage reset LVR
- Power-on reset POR
- Watchdog WDT reset
- Software reset

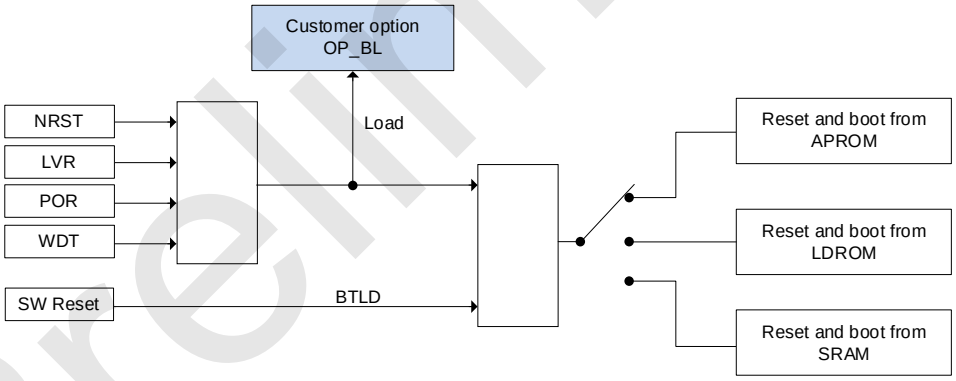
The circuit diagram of the reset part of the SC32F15G is as follows:



SC32F15G Reset Circuit Diagram

6.2.1 Boot area after the reset

After hardware reset through external RST, low voltage reset (LVR), power-on reset (POR), or watchdog reset (WDT), the chip boots from the startup area (APROM / LDROM / SRAM) set by the user in OP_BL. After the software reset, the chip boots from the startup area (APROM / LDROM / SRAM) set by BTLD[1:0].



SC32F15G Boot Area Switching diagram after reset

6.2.2 External RST

External reset is a low-level reset pulse signal of a certain width given to SC32F15G from external RST pin to realize the reset of SC32F15G. User can configure the PC11/NRST pin as RST (reset pin) using the programming host software by Customer Option before programming.

6.2.3 Low-voltage Reset LVR

The SC32F15G provides a low-voltage reset circuit. There are 4-level LVR voltage options: 4.3V, 3.7V, 2.9V, 1.9V. The default value is the Customer Option value written by the user. A reset occurs when the VDD voltage is less than the threshold voltage for low-voltage reset and the duration is greater than T_{LVR}. Among them, T_{LVR} is the buffeting time of LVR, about 30μs.

6.2.4 Power-on Reset(POR)

The SC32F15G has a power-on reset circuit inside. When the power supply voltage V_{DD} reaches the POR reset voltage, the system automatically resets.

6.2.5 Watchdog Reset(WDT)

The SC32F15G has a WDT, the clock source of which is the built-in 32 kHz oscillator. The user can choose whether to enable the watchdog reset function by Customer Option.

6.2.6 Software Reset

Enable RST(IAP_CON.8) will immediately reset the system.

6.2.7 Initial Reset State

When SC32F15G is in the reset state, most registers return to their initial state. The watchdog (WDT) is in the disabled state. 'Hot-start' resets (such as WDT, LVR, software reset, etc.) do not affect SRAM, and SRAM values remain the same as before the reset.

Loss of SRAM content occurs when the power supply voltage drops to a level where RAM cannot retain data.

6.3 Clock

6.3.1 System Clock Source

Three different clock sources can be used to drive the system clock (SYSCLK):

- Built-in high-frequency 72MHz oscillator (HIRC)
- Built-in low-frequency 32kHz oscillator (LIRC)
- External low-frequency crystal oscillator (LXT)

Note：

1. **The default system clock source at power-up is HIRC, and it's frequency is f_{HIRC}/2. Users can switch the clock source through software during normal operation after power-up. Before switching, ensure that the selected clock source is in a stable operating state.**
2. **Regardless of the chosen clock source to switch to, the system clock source must first be switched to HIRC before transitioning to the target clock source.**

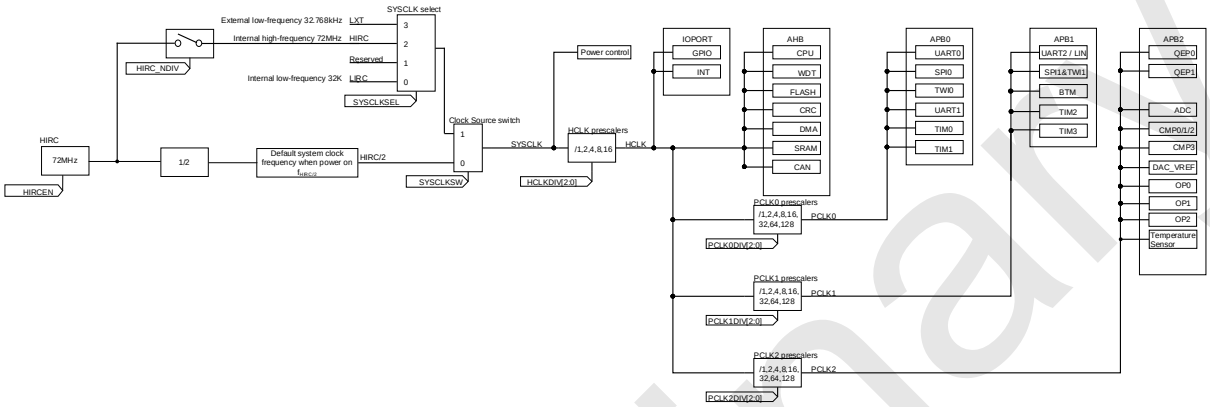
6.3.2 Bus

- Users can configure the frequencies of the AHB, APB0, APB1, and APB2 domains through multiple prescalers.
- HCLK: The main clock of the AHB domain, with a maximum frequency of 72MHz. It drives components such as the Cortex®-M0+ core, memory, and DMA.
- PCLK0: The main clock of the APB0 domain, with a maximum frequency equal to the HCLK frequency. Peripheral devices on the APB0 bus are driven by PCLK0.
- PCLK1: The main clock of the APB1 domain, with a maximum frequency equal to the HCLK frequency. Peripheral devices on the APB1 bus are driven by PCLK1.
- PCLK2: The main clock of the APB2 domain, with a maximum frequency equal to the HCLK

frequency. Peripheral devices on the APB2 bus are driven by PCLK2.

The RCC divides the AHB clock (HCLK) by 8 to serve as the external clock for SysTick. By setting the control and status registers of SysTick, you can choose either the above-mentioned clock or the core clock as the SysTick clock source.

6.3.3 Clock and Bus Allocation Block Diagram



Clock and Bus Allocation Block Diagram

Note: Default system clock frequency when power on "f_{SYS}" is $f_{HIRC/2}$, users can change clock source by modify SYSCLKSW or SYSCLKSEL.

6.4 Built-in high-frequency 72MHz Oscillator (HIRC)

HIRC has the following functions and features:

- Can be selected as the system operating clock
- Default system clock frequency when power on "f_{SYS}" is $f_{HIRC/2}$
- Frequency error: Within ±1% @ -40 to 105℃ @ 2.0V to 5.5V
- The system clock can be automatically calibrated by 32.768 kHz external crystal oscillator, after calibration HIRC accuracy can be infinitely close to the accuracy of external 32.768 kHz crystal oscillator

6.5 Built-in Low-Frequency 32kHz Oscillator (LIRC)

LIRC has the following functions and features:

- Can be selected as the system operating clock
- Can be selected as the Base Timer clock source
- Fixed as the WDT clock source, which will be automaticlly enabled when WDT is enabled
- Frequency error: Within ±4% @ -20 to 85℃ @ 4.0V to 5.5V, after register correction

6.6 External Low-Frequency Oscillator Circuit, Can Connect to 32.768kHz Oscillator (LXT)

LXT has the following functions and features:

- Can be selected as the system operating clock
- Can be selected as the Base Timer clock source
- Allows for an external 32.768kHz low-frequency oscillator
- Automatic calibration of HIRC can be performed using LXT

7 Interrupts

- M0+ core could provide a maximum of 32 interrupt sources, numbered from 0 to 31, while SC32F15G series has 25 interrupt sources.
- Four-level interrupt priorities can be configured, and the interrupt priorities are set through the Interrupt Priority Registers in the core registers.

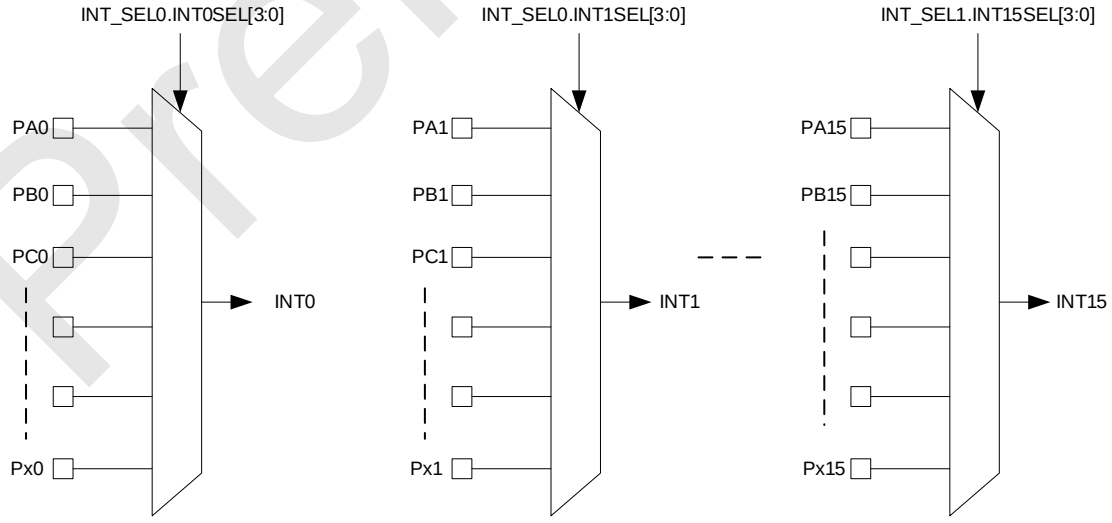
7.1 External interrupts INT0-15

External interrupts comprise 16 interrupt sources, occupying a total of 4 interrupt vectors. All 16 external interrupt sources can be configured to respond to rising edges, falling edges, or both edges. Once configured, these interrupts can cover all GPIO pins. When the corresponding event occurs, software sets the corresponding interrupt flag (RIF/FIF to 1), triggering entry into the corresponding interrupt service.

The external interrupt features of the SC32F15G series are as follows:

- 16 INT interrupt sources, occupying 4 interrupt vectors in total.
- After configuration, INT can cover all GPIO pins.
- All INT sources can be configured for rising edge, falling edge, or both edge interrupts, each having independent corresponding interrupt flag.
- Software sets the corresponding interrupt flag can trigger entry into the corresponding interrupt service.

Note: When using INT functions, users need to manually set the GPIO port corresponding to INTn (n=0-15) to pull-up input mode. External interrupts cannot be detected in output mode.



External Interrupt Port Multiplexer

7.2 Interrupt and Events

- When NVIC is disabled, interrupt request masks are enabled, events can be generated, but interrupt

cannot be generated.

- When NVIC is enabled, interrupt request masks act as internal master interrupt control bit in the module.

7.3 Interrupt Source and Vector

Interrupt Vector	Interrupt Number	Priority	Interrupt Vector Address	Interrupt Source	Core/NVIC Enable Bit	Interrupt Request Mask Bit	Interrupt Subroutine Control Bit	Interrupt Flag	Capability of Waking up STOP
0	-	-	0x0000_0000	-		-	\	\	YES
1	-	Fixed	0x0000_0004	RESET	PRIMASK	SCB	\	\	YES
2	-	Fixed	0x0000_0008	NMI_Handler		SCB	\	\	YES
3	-	Fixed	0x0000_000C	HardFault_Handler	PRIMASK	SCB	\	\	YES
4-10	-	-	0x0000_0010 - 0x0000_0028	-		-	\	\	YES
11	-	Settable		SVC_Handler	PRIMASK	SCB	\	\	YES
12-13	-	-	0x0000_0030 0x0000_0034	-		-	\	\	YES
14	-	Settable	0x0000_0038	PendSV_Handler	PRIMASK	SCB	\	\	YES
15	-	Settable	0x0000_003C	SysTick_Handler	PRIMASK	SysTick_CTRL	\	\	YES
16	0	Settable	0x0000_0040	INT0	NVIC->ISER[0].0	INTF_IE->ENFx，x=0 INTR_IE->ENRx	\	INTF_STS->FIFx INTR_STS->RIFx	YES
17	1	Settable	0x0000_0044	INT1-7	NVIC->ISER[0].1	INTF_IE->ENFx，x=1-7 INTR_IE->ENRx	\	INTF_STS->FIFx INTR_STS->RIFx	YES
18	2	Settable	0x0000_0048	INT8-11	NVIC->ISER[0].2	INTF_IE->ENFx，x=8-11 INTR_IE->ENRx	\	INTF_STS->FIFx INTR_STS->RIFx	YES
19	3	Settable	0x0000_004C	INT12-15	NVIC->ISER[0].3	INTF_IE->ENFx，x=12-15 INTR_IE->ENRx	\	INTF_STS->FIFx INTR_STS->RIFx	YES
20	4	Reserved	0x0000_0050	\	NVIC->ISER[0].4	\	\	\	
21	5	Reserved	0x0000_0054	\	NVIC->ISER[0].5	\	\	\	
22	6	Settable	0x0000_0058	BTM	NVIC->ISER[0].6	BTM_CON->INTEN	\	BTM_STS->BTMIF	YES
23	7	Settable	0x0000_005C	UART0	NVIC->ISER[0].7	UART0_IDE->INTEN	UART0_IDE->TXIE UART0_IDE->RXIE	UART0_STS->TXIF UART0_STS->RXIF	YES
				UART2/LIN		UART2_IDE->INTEN	UART2_IDE->TXIE UART2_IDE->RXIE UART2_IDE->BKIE UART2_IDE->SLVHEIE	UART2_STS->TXIF UART2_STS->RXIF UART2_STS->BKIF UART2_STS->SLVHEIF	NO
24	8	Settable	0x0000_0060	UART1	NVIC->ISER[0].8	UART1_IDE->INTEN	UART1_IDE->TXIE UART1_IDE->RXIE	UART1_STS->TXIF UART1_STS->RXIF	YES
25	9	Settable	0x0000_0064	SPI0	NVIC->ISER[0].9	SPI0_IDE->INTEN	SPI0_IDE->RXNEIE SPI0_IDE->TBIE SPI0_IDE->RXIE	SPI0_STS->SPIF SPI0_STS->RXNEIF SPI0_STS->TXEIF	NO

Interrupt Vector	Interrupt Number	Priority	Interrupt Vector Address	Interrupt Source	Core/NVIC Enable Bit	Interrupt Request Mask Bit	Interrupt Subroutine Control Bit	Interrupt Flag	Capability of Waking up STOP
							SPI0_IDE->RXHIE SPI0_IDE->TXHIE	SPI0_STS->RXFIF SPI0_STS->RXHIF SPI0_STS->TXHIF	
26	10	Settable	0x0000_0068	SPI1	NVIC->ISER[0].10	SPI1_TWI1_IDE->INTEN	SPI1_TWI1_IDE->TBIE	SPI1_TWI1_STS->QTWIF SPI1_TWI1_STS->TXEIF	NO
				TWI1				SPI1_TWI1_STS->QTWIF	NO
27	11	Settable	0x0000_006C	DMA0	NVIC->ISER[0].11	DMA0_CFG->INTEN	DMA0_CFG->TCIE DMA0_CFG->HTIE DMA0_CFG->TEIE	DMA0_STS->GIF DMA0_STS->TCIF DMA0_STS->HTIF DMA0_STS->TEIF	NO
28	12	Settable	0x0000_0070	DMA1	NVIC->ISER[0].12	DMA1_CFG->INTEN	DMA1_CFG->TCIE DMA1_CFG->HTIE DMA1_CFG->TEIE	DMA1_STS->GIF DMA1_STS->TCIF DMA1_STS->HTIF DMA1_STS->TEIF	NO
29	13	Settable	0x0000_0074	DMA2	NVIC->ISER[0].13	DMA2_CFG->INTEN	DMA2_CFG->TCIE DMA2_CFG->HTIE DMA2_CFG->TEIE	DMA2_STS->GIF DMA2_STS->TCIF DMA2_STS->HTIF DMA2_STS->TEIF	NO
30	14	Settable	0x0000_0078	DMA3	NVIC->ISER[0].14	DMA3_CFG->INTEN	DMA3_CFG->TCIE DMA3_CFG->HTIE DMA3_CFG->TEIE	DMA3_STS->GIF DMA3_STS->TCIF DMA3_STS->HTIF DMA3_STS->TEIF	NO
31	15	Settable	0x0000_007C	TIM0	NVIC->ISER[0].15	TIM0_IDE->INTEN	TIM0_IDE->TIE TIM0_IDE->EXFIE TIM0_IDE->EXRIE	TIM0_STS->TIF TIM0_STS->EXIF TIM0_STS->EXIR	NO
32	16	Settable	0x0000_0080	TIM1	NVIC->ISER[0].16	TIM1_IDE->INTEN	TIM1_IDE->TIE TIM1_IDE->EXFIE TIM1_IDE->EXRIE	TIM1_STS->TIF TIM1_STS->EXIF TIM1_STS->EXIR	NO
33	17	Settable	0x0000_0084	TIM2	NVIC->ISER[0].17	TIM2_IDE->INTEN	TIM2_IDE->TIE TIM2_IDE->EXFIE TIM2_IDE->EXRIE	TIM2_STS->TIF TIM2_STS->EXIF TIM2_STS->EXIR	NO
34	18	Settable	0x0000_0088	TIM3	NVIC->ISER[0].18	TIM3_IDE->INTEN	TIM3_IDE->TIE TIM3_IDE->EXFIE TIM3_IDE->EXRIE	TIM3_STS->TIF TIM3_STS->EXIF TIM3_STS->EXIR	NO
35	19	Reserved	0x0000_008C	\	NVIC->ISER[0].19	\	\	\	

Interrupt Vector	Interrupt Number	Priority	Interrupt Vector Address	Interrupt Source	Core/NVIC Enable Bit	Interrupt Request Mask Bit	Interrupt Subroutine Control Bit	Interrupt Flag	Capability of Waking up STOP
36	**20**	Settable	0x0000_0090	QEP0	NVIC->ISER[0].20	QEP0_IDE->INTEN	QEP0_IDE->PCUIE QEP0_IDE->PCOIE QEP0_IDE->IERIE QEP0_IDE->UPEVNTIE	QEP0_STS->PCUIF QEP0_STS->PCOIF QEP0_STS->IERIF QEP0_STS->UPEVNTIF	NO
37	**21**	Settable	0x0000_0094	\	NVIC->ISER[0].21	\	\	\	
38	**22**	Settable	0x0000_0098	OP1_CMP	NVIC->ISER[0].22	OP_IDE>INTEN	OP_IDE->OP_CMP1IE	OP_STS->OP_CMP1IF	NO
				OP2_CMP			OP_IDE->OP_CMP2IE	OP_STS->OP_CMP2IF	NO
39	**23**	Settable	0x0000_009C	TWI0	NVIC->ISER[0].23	TWI0_IDE->INTEN	\	TWI0_STS->TWIF	NO
40	**24**	Settable	0x0000_00A0	QEP1	NVIC->ISER[0].24	QEP1_IDE->INTEN	QEP1_IDE->PCUIE QEP1_IDE->PCOIE QEP1_IDE->IERIE QEP1_IDE->UPEVNTIE	QEP1_STS->PCUIF QEP1_STS->PCOIF QEP1_STS->IERIF QEP1_STS->UPEVNTIF	NO
41	**25**	Reserved	0x0000_00A4	\	\	\	\	\	
42	**26**	Reserved	0x0000_00A8	\	\	\	\	\	
43	**27**	Reserved	0x0000_00AC	\	\	\	\	\	
44	**28**	Settable	0x0000_00B0	**CAN**	NVIC->ISER[0].28	CAN_IDE->INTEN	CAN_RTIE->RIE CAN_RTIE->ROIE CAN_RTIE->RFIE CAN_RTIE->RAFIE CAN_RTIE->TPIE CAN_RTIE->TSIE CAN_RTIE->EIE CAN_RTIE->EPIE CAN_RTIE->ALIE CAN_RTIE->BEIE	CAN_RTIE->RIF CAN_RTIE->ROIF CAN_RTIE->RFIF CAN_RTIE->RAFIF CAN_RTIE->TPIF CAN_RTIE->TSIF CAN_RTIE->EIF CAN_RTIE->EPIF CAN_RTIE->ALIF CAN_RTIE->BEIF	NO
45	**29**	Settable	0x0000_00B4	ADC	NVIC->ISER[0].29	ADC_CON->INTEN	ADC_IDE->EOCIE ADC_IDE->EOSIE0 ADC_IDE->EOSIE1 ADC_IDE->EOSIE2 ADC_IDE->EOSIE3 ADC_IDE->UPTHIE ADC_IDE->DOWTHIE	ADC_STS->EOCIF ADC_STS->EOSIF0 ADC_STS->EOSIF1 ADC_STS->EOSIF2 ADC_STS->EOSIF3 ADC_STS->UPTHIF ADC_STS->DOWTHIF	NO
46	**30**	Settable	0x0000_00B8	CMP0	NVIC->ISER[0].30	CMPX_IDE->INTEN	CMPX_IDE->CMP0IE	CMPX_STS->CMP0IF	YES

Interrupt Vector	Interrupt Number	Priority	Interrupt Vector Address	Interrupt Source	Core/NVIC Enable Bit	Interrupt Request Mask Bit	Interrupt Subroutine Control Bit	Interrupt Flag	Capability of Waking up STOP
				CMP1			CMPX_IDE->CMP1IE	CMPX_STS->CMP1IF	
				CMP2			CMPX_IDE->CMP2IE	CMPX_STS->CMP2IF	
47	**31**	Settable	0x0000_00BC	CMP3	NVIC->ISER[0].31	CMP3_IDE->INTEN	\	CMP3_STS->CMP3IF	YES

8 Analog-to-Digital Converter(ADC)

8.1 Overview

The SC32F15G series features a 12-bit successive approximation type analog-to-digital converter (ADC). It supports up to 18 multiplexed channels which can measure signals from 16 external sources and 2 internal sources(VDD and chip temperature). The A/D conversion for each channel can be performed in single-shot or continuous sampling modes. The results of the ADC are stored in a 32-bit data register.

8.2 Clock Source

- The SC32F15G series ADC has only one clock source, which is derived from PCLK
- Typcial conversion time: 404ns

8.3 Feature

- Precision：12 bits
- Maximum Channels: Supports up to 18 channels:
  - External 16 ADC sampling channels can be multiplexed with I/O ports for other function
  - Output port of OP0,OP1,OP2 are multiplexed with ADC channels, and the output value can be directly read through ADCV register
  - One internal ADC can directly measure VDD voltage
  - One internal temperature sample channel
- Configurable ADC upper and lower threshold, which can trigger interrupt
- Selectable trigger mode:
  - Manual single trigger
  - Sequential trigger(Only available through software trigger)
- Configurable ADC conversion completion interrupt
- Single-channel conversion time:404ns
- Supports DMA transmission: DMA request will be generated after ADC conversion complete
- The conversion results feature an overflow flag: OVERRUN, and the OVERRUN flag bit is located in the same register as the ADC conversion results so users can read the information all at once.

8.4 ADC Sampling and Conversion Time

LOWSP[2:0] Value	Sampling cycle	Sampling time @F_{PCLK} = 72MHz unit:ns	Conversion time unit:ns	Totol time unit:ns
000	3	42	404	446
001	6	83	404	487
010	9	125	404	529

LOWSP[2:0] Value	Sampling cycle	Sampling time @F_{PCLK} = 72MHz unit:ns	Conversion time unit:ns	Totol time unit:ns
011	15	208	404	612
100	30	417	404	821
101	60	833	404	1237
110	120	1667	404	2071
111	480	6667	404	7071

8.5 ADC Conversion Steps

The actual operation steps required for the user to perform ADC conversion are as follows:

① Set the ADC input pin; (set the bit corresponding to AINx as ADC input, usually the ADC pin will be fixed in advance);

② Set the ADC reference source using the REFSEL bit: If VREF is selected, the reference value for VREF must be configured separately.

③ Enable the ADC module power: Write 1 to the ADCEN bit to power on the ADC module.

④ Set ADCISA[4:0]: Select the idle channel for manual trigger sampling.

⑤ Configure upper and lower thresholds using UPTH[11:0] and DOWTH[11:0]: If the ADC conversion result exceeds the thresholds, the corresponding flag will be set. Additionally, users can configure whether threshold comparison is enabled for each channel via the ADC_TH_CFG register

⑥ Choose single or sequence conversion mode:

- For single conversion, set CONT to 0 and write 1 to ADCS to trigger the conversion for the channel selected by ADCISA.
- For sequence conversion, pre-configure the sequence order in the ADC_SQ0 register, set the starting position of the sequence using SQSTR0 in the ADC_SQCNT register and the number of samples using SQCNT0, to start sequence conversion, set CONT to 1 and write 1 to ADCS. The conversion will proceed in ascending order based on the valid DSn numbers in the sequence.

⑦ ADCIF flag indicates completion of a conversion: If ADC interrupts are enabled and EOCIE is set, a conversion completion interrupt will be triggered. The user must clear the ADCIF flag in software.

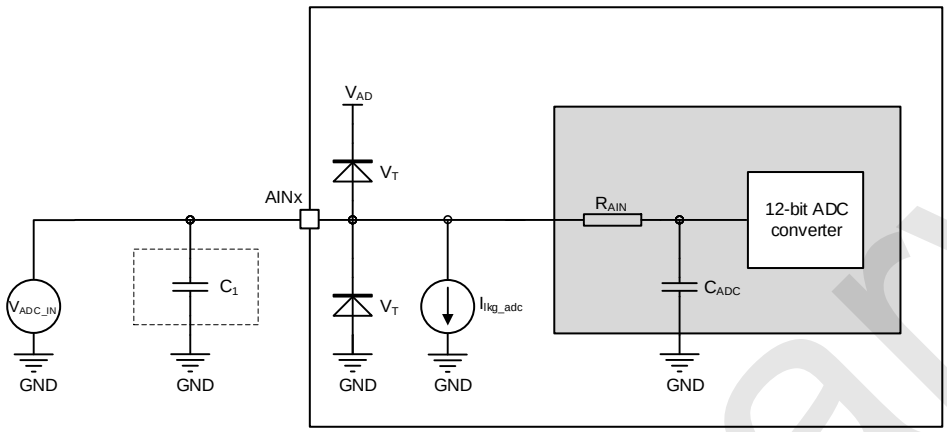
⑧ EOSIF0 flag indicates completion of a sequence conversion: If ADC interrupts are enabled and EOSIE0 is set, a sequence completion interrupt will be triggered. The user must clear the EOSIF0 flag in software

⑨ In sampling mode, the conversion result for the sampled channel is stored in ADCVA[11:0]: If the ADCV register is not read in time, the next conversion result will overwrite the current one, and the OVERRUN bit will be set to indicate overflow. Overflow does not affect sampling or conversion. The OVERRUN bit will be automatically cleared when the ADCV register is read

⑩ If ADC conversion thresholds are set: After the conversion result is stored in ADCVA[11:0], it will be compared with the upper and lower thresholds. If the result exceeds the thresholds, the UPTHIF (upper threshold overflow flag) or DOWTHIF (lower threshold overflow flag) will be set. If ADC interrupts are enabled and UPTHIE/DOWTHIE is set, a threshold overflow interrupt will be triggered.

⑪ DMA can be used to transfer conversion data.

8.6 ADC Structure Diagram



Note:

1. **C1 is an external 0.01μF capacitor. Users are advised to add this capacitor to improve the performance of the ADC.**
2. **For detailed electrical parameters related to the ADC, please refer to Section 27.9 ADC Characteristics.**

9 Internal Reference Source(VREF)

9.1 Overview

The SC32F15G series features an independent internal reference source(VREF), and can be reference source of some peripherals.

9.2 Clock Source

- The SC32F15G series VREF has only one clock source, which is derived from PCLK2

9.3 Internal Reference Source Configuration

There are four methods to configure internal reference source module:

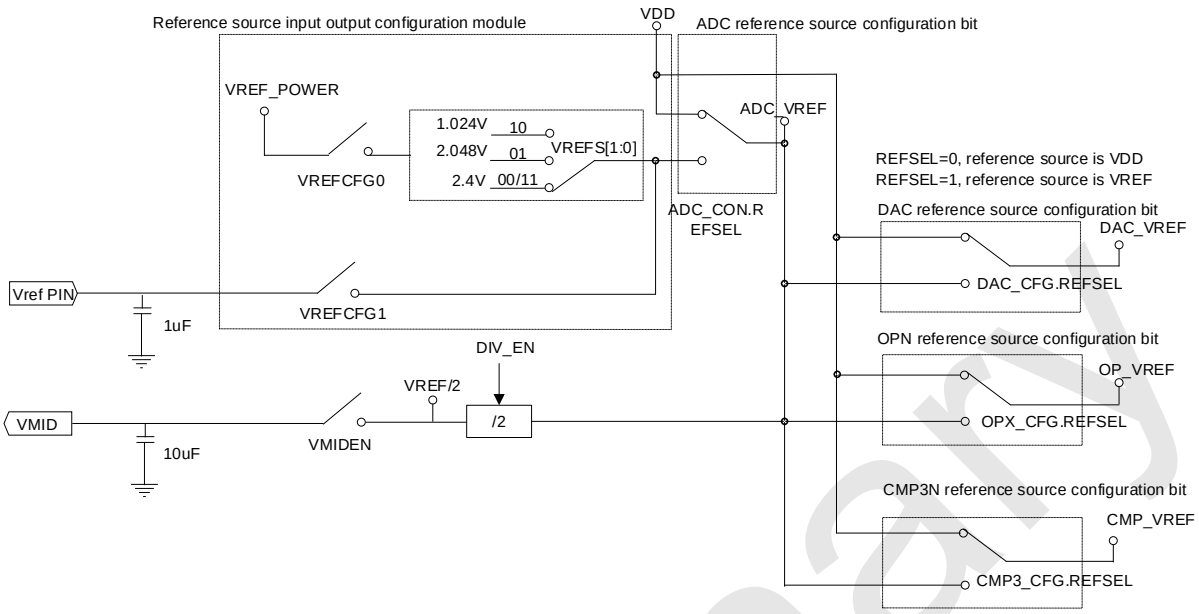
- VREFCFG1=0,VREFCFG0=0: disable Vref PIN port, disable internal reference source module
- VREFCFG1=0,VREFCFG0=1: the analog circuit uses the internal reference, and the Vref voltage is determined by the VREFS[1:0] selection.
- VREFCFG1=1,VREFCFG0=0: the analog circuit uses an external reference, and Vref is input through the external Vref PIN.
- VREFCFG1=1,VREFCFG0=1: the analog circuit uses the internal reference, and the Vref voltage is determined by the VREFS[1:0] selection.

9.4 Internal Reference Source Output

Once the internal reference source module is enabled, VREF can be utilized as a reference for ADC, DAC, OP, or CMP. Additionally, it can be divided by two and output through the VMID pin.

9.5 Internal Reference Source Structure Diagram

Vref PIN can be used as input port, and VMID can be only used as output port



10 Digital-to-Analog Converter(DAC)

10.1 Overview

The SC32F15G series features an independent digital-to-analog converter(DAC). The DAC features two independent output ports, DACOUT0 and DACOUT1. Additionally, the DAC can internally route its output to the inverting input port of OP1 or OP2.

10.2 Clock Source

- The SC32F15G series DAC has only one clock source, which is derived from PCLK2

10.3 Feature

- Reference source selectable: VDD or VREF
- Output ports:
  - 2 independent DAC output port DACOUT0 and DACOUT1
  - Inverting input port of OP1/OP2
  - Negative port of CMP0/1/2/3

11 Temperature Sensor

11.1 Overview

The SC32F15G series features a temperature sensor, and temperature sensor voltage can be measured though ADC.

11.2 Temperature Sensor Operation Step

When using the temperature sensor, the ADC reference voltage should be set to the internal 2.4V reference. For every 1°C increase in temperature, the ADC conversion value will increase by a fixed amount. SinOne has pre-programmed the ADC conversion result corresponding to 25°C for each chip into a specific address during production.

The steps for operating the temperature sensor are as follows:

① Set the ADC reference voltage (Vref) to the internal 2.4V reference source and configure the ADC sampling period. It is recommended to select a sampling clock of 60 or more cycles. Then, enable the ADC module power.
② Select the ADC input channel as the temperature sensor channel.
③ Enable the temperature sensor by setting TS_EN to 1.
④ Wait for a delay of 20μs.
⑤ Set TS_CHOP to 0 to initiate the first ADC conversion. Once the conversion is complete, record the conversion value as ADC_{Value1}.
⑥ Set TS_CHOP to 1 to initiate the second ADC conversion. Once the conversion is complete, record the conversion value as ADC_{Value2}.
⑦ Calculate the average of the two conversion values:

$$ADC_{Value} = \frac{(ADC_{Value1} + ADC_{Value2})}{2}$$

⑧ Read the factory-programmed ADC conversion value for 25°C ($ADC_{ValueTest}$) from the corresponding address.
⑨ Substitute the values into the formula to calculate the current temperature:

$$Temperature = 25℃ + \frac{(ADC_{Value} - ADC_{ValueTest})}{8.53}$$

For more detailed information about the temperature sensor, please refer to the “SinOne SC32F1XXX Series MCU Application Guide V1.4”.

12 Operational Amplifier(OP)

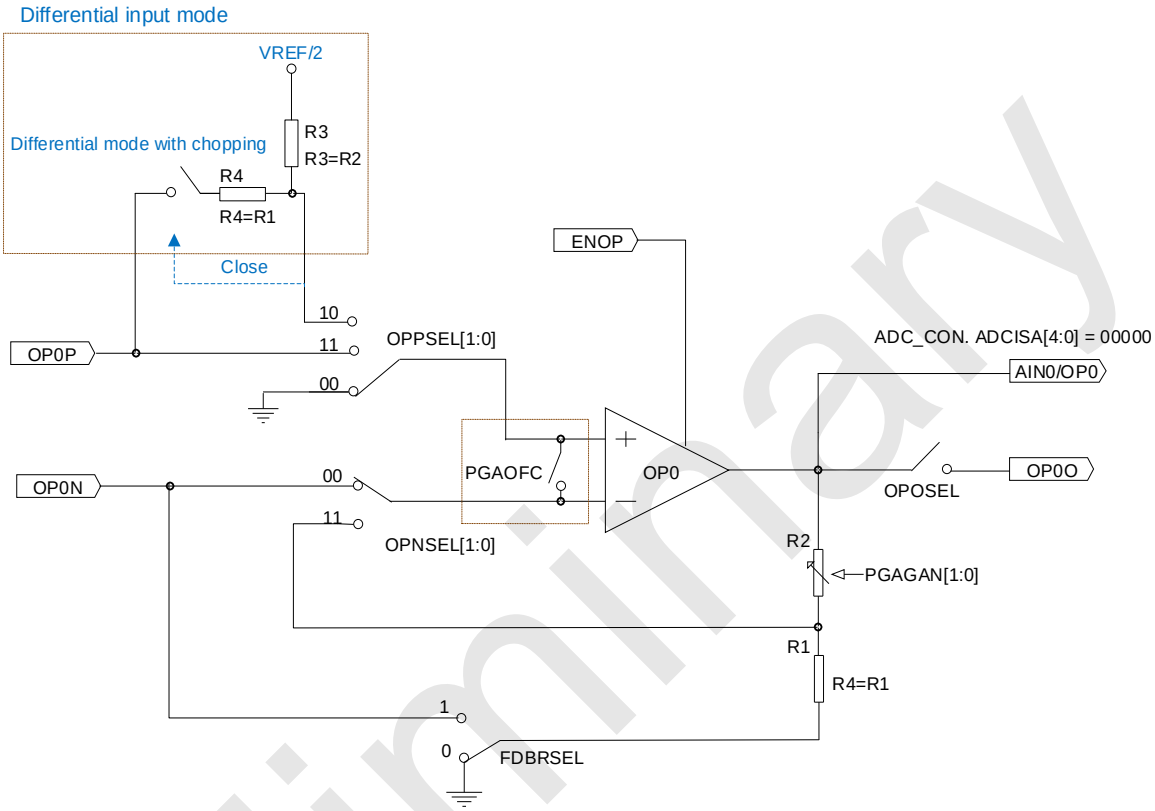
12.1 Overview

The SC32F15G series features 3 independent rail-to-rail operational amplifiers:OP0/OP1/OP2.

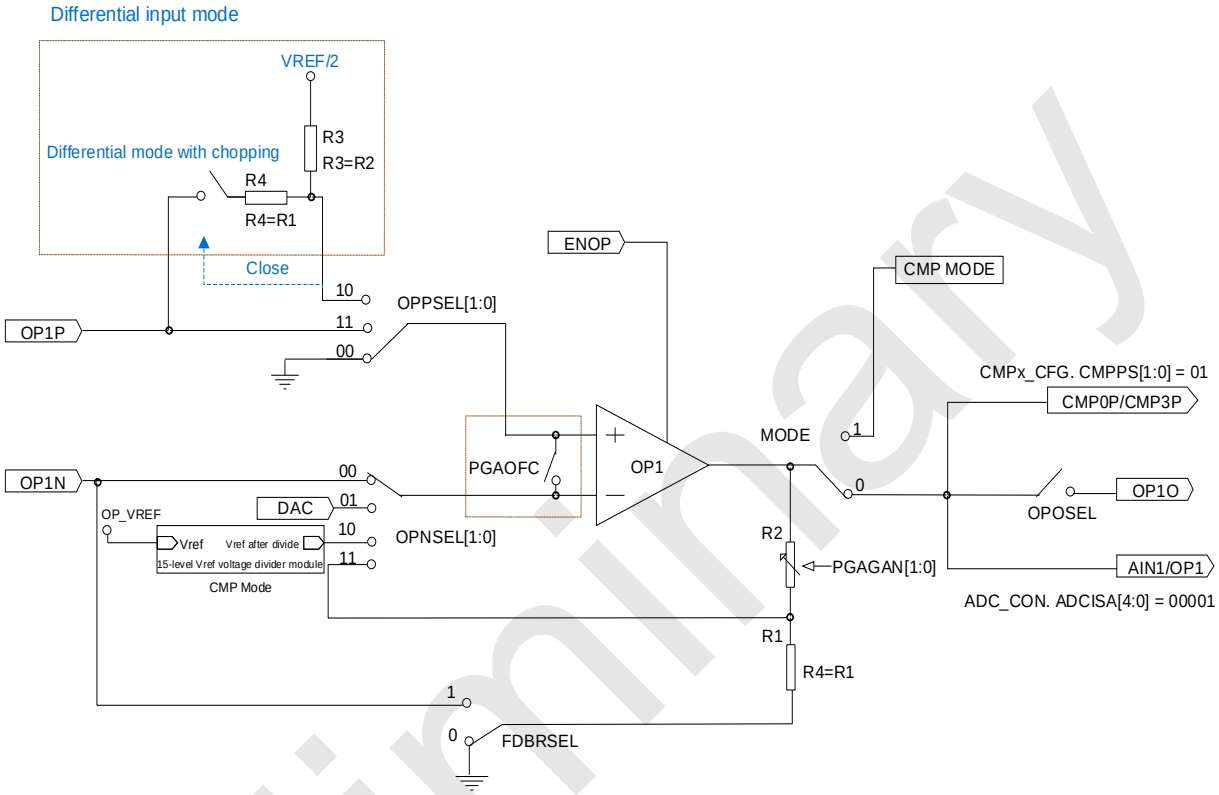
12.2 Feature

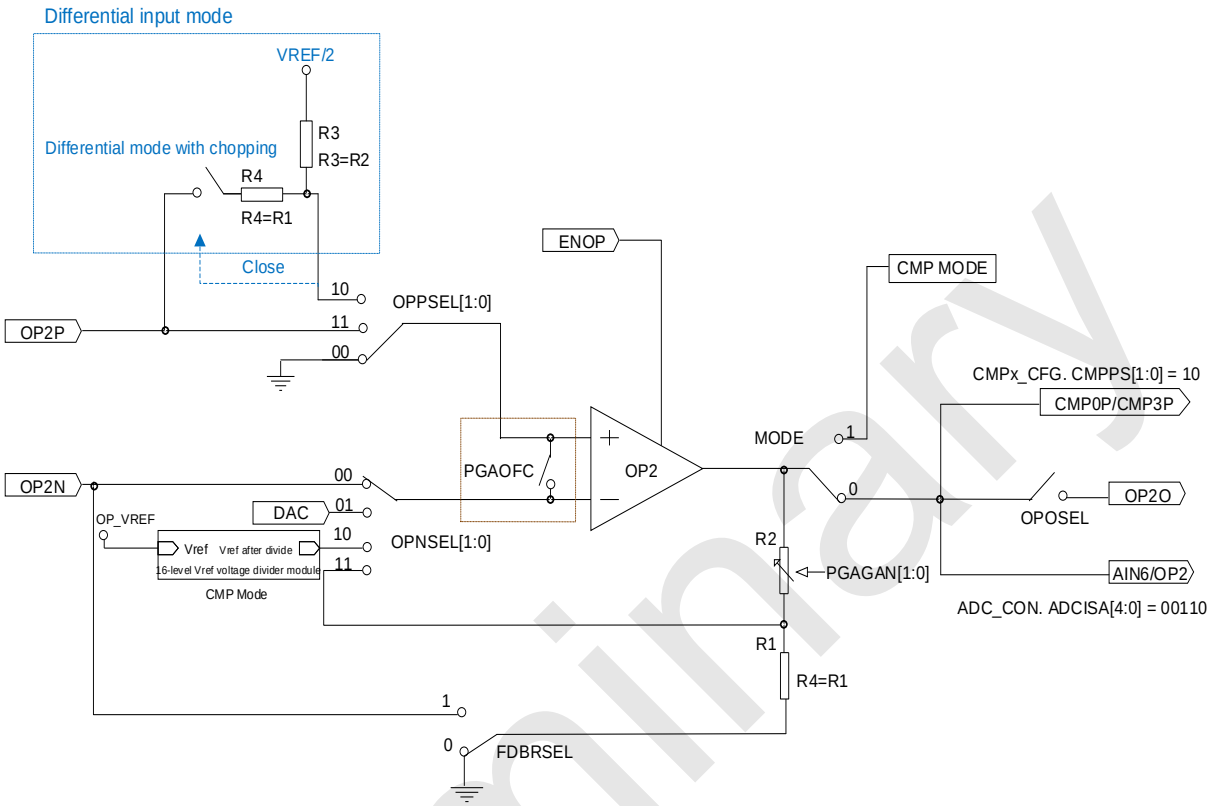
- All three OPs can be configurable as a Programmable Gain Amplifier (PGA)
  - Non-inverting gain: 4/8/16/32
  - Inverting gain: 3/7/15/31
- All three OPs have independent non-inverting input port, inverting input port and output port
- Output port of OP0,OP1,OP2 are multiplexed with ADC channels, and the output value can be directly read through ADCV register
- OP1/OP2 can be configurable as CMP
  - Comparator voltage hysteresis: 10-15mV
  - Response time: typical 50ns
- The output of OP1/OP2 can be directly connected to the positive input of CMP0 and CMP3
  - Bandwidth 10MHz
  - Offset voltage≤10mV, and need zero calibration
  - Slew rate≥10V/us

12.3 OP0 Structure Diagram



12.4 OP1/OP2 Structure Diagram





12.5 OP0 Port Selection

12.5.1 OP0 Accuracy Adjustment

The accuracy of OP0 can be adjusted by enabling the PGA offset adjustment control bit (PGAOFC). This is achieved by shorting the positive and negative input terminals of the OP module internally. This process helps to calibrate and minimize any offset errors in the operational amplifier. After calibration, set PGAOFC = 0 to disable the offset adjustment mode and restore normal operation of the OP module.

12.5.2 OP0 Non-Inverting Input Selection

The non-inverting input terminal of OP0 module can be switched and selected by OPPSEL[1:0], and it has three options:

- OP0P external pin
- Internal VSS
- Differential input mode

When differential mode is selected, it is necessary to simultaneously enable the DIV_EN bit in the VREF_CFG register to ensure that the bias voltage $V_{REF}/2$ is output.

12.5.3 OP0 Inverting Input Selection

The inverting input terminal of the OP0 module has two options:

- OP0N external pin.

When choosing the OP0N external pin as the inverting input for the OP0, the OP0 input control bit OPNSEL[1:0] should be set to 00, and the feedback resistor selection bits FDBRSEL should be set to 1.

- Internal feedback resistor.

When choosing the internal feedback resistor as the inverting input for the OP0, the OP0 input control bit OPNSEL[1:0] should be set to 11, and the feedback resistor selection bits FDBRSEL should be set to 0 or 1, and the internal gain can be selected by internal gain selection bits PGAGAN[1:0].

12.5.4 OP0 Output Selection

The output of the OP0 module has two options:

- Sampling channel of the AD converter

When OP0 output is used as an ADC input, users should set ENOP=1 to enable the OP module, then set ADCEN=1 to power on the ADC. The conversion result of OP can be directly obtained in the ADCV register by selecting the OP output port as the ADC input port through setting ADCISA[4:0]=00000.

- OP0O pin.

When OP outputs through the OP0O pin,users should set ENOP=1 to enable the OP module,then set OPOSEL=1

12.6 OP1/2 Port Selection

12.6.1 OP1/2 Accuracy Adjustment

The accuracy of OP1/2 can be adjusted by enabling the PGA offset adjustment control bit (PGAOFC). This is achieved by shorting the non-inverting and inverting input terminals of the OP module internally. This process helps to calibrate and minimize any offset errors in the operational amplifier. After calibration, set PGAOFC = 0 to disable the offset adjustment mode and restore normal operation of the OP module.

12.6.2 OP1/2 Non-Inverting Input Selection

The non-inverting input terminal of OP1/2 module can be switched and selected by OPPSEL[1:0], and it has three options:

- OP1P/OP2P external pin
- Internal VSS
- Differential input mode

When differential mode is selected, it is necessary to simultaneously enable the DIV_EN bit in the VREF_CFG register to ensure that the bias voltage $V_{REF}/2$ is output.

12.6.3 OP1/2 Inverting Input Selection

The inverting input terminal of the OP1/2 module has four options:

- OP1N/OP2N external pin.

When choosing the OP1N/OP2N external pin as the inverting input for the OP1/2, the OP1/2 input control

bit OPNSEL[1:0] should be set to 00, and the feedback resistor selection bits FDBRSEL should be set to 1.

- DAC output

When choosing the DAC output as the inverting input for the OP1/2, the DAC module must be enabled and the OP1/2 input control bit OPNSEL[1:0] should be set to 01

- 15-level voltage divider of OPx_VREF

When choosing the OPRF[3:0] as the inverting input for the OP1/2, the OP1/2 input control bit OPNSEL[1:0] should be set to 10

- Internal feedback resistor.

When choosing the internal feedback resistor as the inverting input for the OP0, the OP1/2 input control bit OPNSEL[1:0] should be set to 11, and the feedback resistor selection bits FDBRSEL should be set to 0 or 1, and the internal gain can be selected by internal gain selection bits PGAGAN[1:0].

12.6.4 OP1/2 Output Selection

The output of the OP module has three options:

- Sampling channel of the AD converter

When OP1/2 output is used as an ADC input, users should set ENOP=1 to enable the OP module and set MODE=0 to configure OP1/2 as amplifer mode, then set ADCEN=1 to power on the ADC. The conversion result of OP can be directly obtained in the ADCV register by selecting the OP output port as the ADC input port through setting ADCISA[4:0]=00001/00110.

- Non-inverting input of the CMP0/3

When OP1/2 is used as the non-inverting input of the CMP0/3, users should set ENOP=1 to enable the OP module, then select OP output port as the CMP input port by channel control bit CMPPS[1:0].

- OP1O/OP2O pin.

When OP outputs through the OP1O/OP2O pin,users should set ENOP=1 to enable the OP module,then set OPOSEL=1

13 Analog Comparator(CMP)

13.1 Overview

The SC32F15G series features 4 built-in analog comparators (CMP), CMP0/1/2 shared the negative input port and CMP3 is completely independent.

CMP interrupt can wake up the STOP Mode. It can be used for applications such as alarm circuits, power supply voltage monitoring circuits, zero-crossing detection circuits, etc.

13.2 Clock Source

- The SC32F15G series CMP has only one clock source, which is derived from PCLK2

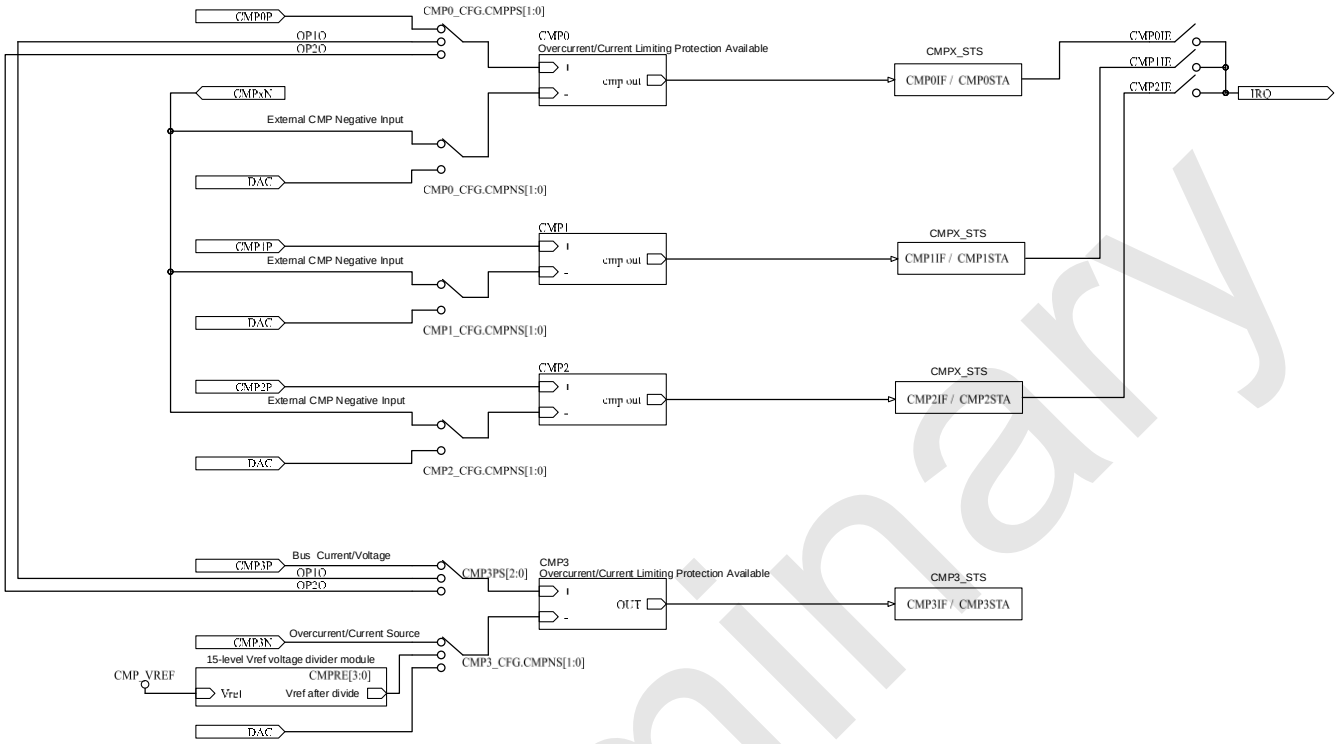
13.3 CMP0/1/2 Feature

- CMP0/1/2 have indenpendent external input port
- Positive input of CMP0 can select the output of OP1 and OP2
- Negative input of CMP0/1/2 selectable:
  - Shared input port CMPxN
  - Internal DAC output
- CMP0/1/2 interrupts can wake up the STOP mode
- Comparator voltage hysteresis: 0/5/10/20mV
- Response time: typical 50ns

13.4 CMP3 Feature

- Positive input of CMP3 selectable:
  - External input port CMP3P
  - Internal OP1 or OP2 output
- Negative input of CMP3 selectable:
  - External input port CMP3N
  - Internal DAC output
  - 16-level Vref voltage divider module output
- CMP3 interrupts can wake up the STOP mode
- Comparator voltage hysteresis: 0/5/10/20mV
- Response time: typical 50ns

13.5 Analog Comparator Structure Diagram



Analog Comparator Structure Diagram

14 Quadrature Encoder Pulse (QEP) Module

14.1 Overview

The SC32F15G series features 2 QEP modules, they can be connected to linear or rotary incremental encoders to obtain machine position, direction, and speed information.Users can configure the QSRC[1:0] bit in QEPn_CON (n=0-1) register to select the counting method.

The SC32F15G series provides 3 counting method: Quadrature Counting, Direction Counting and Dual Pulse Counting.

14.2 Feature

- Each QEPn module (n = 0-1) provides three input signal pins: QEPnA, QEPnB and QEPnI
  - QEPnA and QEPnB can be swapped in direction
  - The polarity of QEPnA and QEPnB can be individually configured
  - Provides a configurable digital filter with a maximum division factor of 128 for QEPnA, QEPnB, and QEPnI signals
- In Direction Counting and Dual Pulse Counting modes, counting can be configured for:
  - Rising edge
  - Falling edge
  - Both edges (rising and falling)
- Position Counter Reset Modes:
  - Index Event Reset
  - overflow Reset(When PCNT=PMAX)

14.3 Counting Method

- Quadrature Counting
- Direction Counting
- Dual Pulse Counting

15 16-bit Timers (Timer0-Timer3)

15.1 Clock Source

- In timer mode/PWM output mode, the TIM clock source is derived from PCLK
- In counter mode, the Tn pin serves as the counting source input

15.2 Feature

- Supports 8-stage TIM clock pre-scaling
- 4 independent 16-bit auto-reload counters: Timer0 to Timer3
- 16-bit incremental, decremental, and increment/decrement auto-reload counters
- Support rising/falling edge capture, enabling PWM duty and period capture
- Overflow and capture events of TIM1/2 can generate DMA requests
- All timer pins(Tn and TnEX) can be remapped

15.3 Counting method

15.3.1 Counting Method in Timer Mode

- Upward Counting: Counts from the set value upwards to overflow at 0xFFFF
- Downward Counting: Counts from 0xFFFF downwards to the set value

15.3.2 Counting Method in PWM Mode

Only upward counting mode is available in PWM output mode: The counter starts from 0 and counts up until PDT, then PWM output waveform will switch between the high and low levels. The counting will then continue up to RLD, causing an overflow and the counter reset to 0.

The formula of TPWM is shown as follows:

$$T_{PWM} = \frac{RLD[15:0] + 1}{PCLK}$$

The formula of duty is shown as follows:

$$duty = \frac{PDT[15:0]}{RLD[15:0] + 1}$$

15.4 Timer Signal Port

- Tn, n=0-3
  - Clock input/output
  - Both rising and falling edges can be captured
- TnEX, n=0-3
  - In reload mode, the external event input (falling edge) on the TnEX pin is used for reload

enable/disable control

- In capture mode, when FSEL = 1, it serves as a falling edge capture signal input. Detection of a falling edge on the TnEX pin generates a capture, sets EXIF, and captures the value of the TnCNT register into the FCAP register

- TnPWM, n=0-3
  - TIM0-3 can provide PWM with independently adjustable duty cycle through the Tn port: TnPWMA
  - TIM0-3 can provide PWM with independently adjustable duty cycle through the TnEX port: TnPWMB
  - Optional clock source follows TIM
  - Note: TIM's PWM capture function and PWM output function cannot be enabled simultaneously

15.5 Interrupts and Corresponding Flags for TIM

- Overflow/underflow of the counter share the interrupt flag TIF
- Capture status flags:
  - EXIF: Flag indicating detection of a falling edge on the external event input
  - EXIR: Flag indicating detection of a rising edge on the external event input
- Interrupt and priority configuration control bits are merged into the NVIC module

16 Power Saving Mode

Upon initial power-up, the system runs in Normal Mode. Additionally, three power-saving modes are available:

- Low-Speed Mode: The system clock source can be LIRC, and the CPU can operate at 32kHz.
- IDLE Mode: The system can be awakened by any interrupt.
- STOP Mode: The system can be awakened by INT0-15, Base Timer and CMP.

17 GPIO

17.1 Clock Source

M0+ core can achieve single-cycle access to GPIO through the IOPORT bus, resulting in highly efficient data transfer. The IOPORT bus clock is derived from HCLK.

17.2 Feature

The GPIO port features of the SC32F15G series are as follows:

- A maximum of 45 bidirectional independently controlled GPIOs
- CPU can access GPIO ports through the IOPORT bus in a single cycle
- Independent setting of pull-up resistors
- All ports have four levels of source driving capability
- All I/Os have high sink current driving capability (50mA)
- 16 I/Os in one group
- Whether input mode or output mode, reading from the port data register retrieves the actual status value of the port

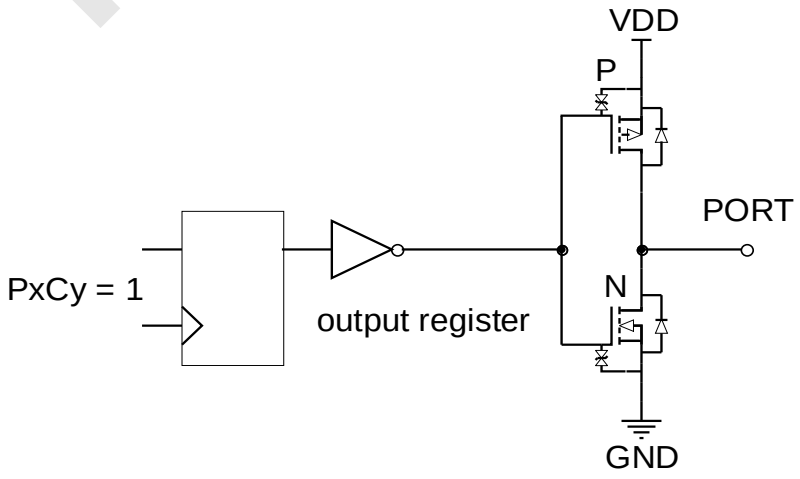
Note: Unused and non-exported ports should be set to strong push-pull output mode

17.3 GPIO Structure Diagram

Strong Push-pull Output Mode

In the strong push-pull output mode, it can provide continuous high-current drive: For detailed electrical parameters, please refer to the "GPIO Parameters" section.

The schematic diagram of the port structure of the strong push-pull output mode is as follows:

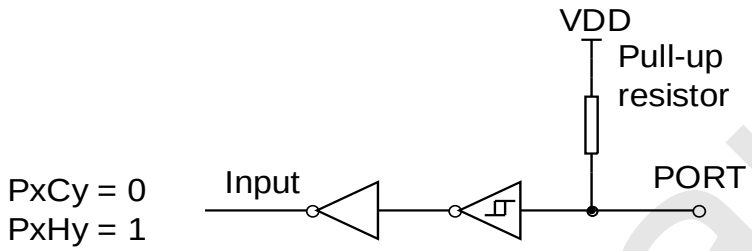


Strong push-pull output mode

Pull-up Input Mode

In the pull-up input mode, a pull-up resistor is constantly connected to the input port. Only when the input port is pulled low, the low-level signal is detected.

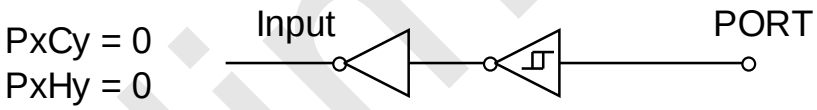
The schematic diagram of the port structure with pull-up input mode is as follows:



Input mode with pull-up resistor

High Impedance Input Mode (Input only)

The schematic diagram of the port structure of the high impedance input mode is as follows:



High impedance input mode

18 UART0-2

18.1 Clock Source

The SC32F15G series UART has only one clock source, which is derived from PCLK

18.2 Feature

- Three UARTs，UART0-2
- UART2 has a complete LIN interface
  - Can switch between master and slave modes
  - Supports hardware break sending in master mode (10/13 bits)
  - Supports hardware break detection in slave mode (10/11 bits)
  - Supports baud rate synchronization in slave mode
  - Provides related interrupts/status bits/flags/fault tolerance range
- UART0-2 support signal port mapping and can be mapped to another set of I/Os
- Each UART has four communication modes to choose from:
  - Mode 0: 8-bit half-duplex synchronous communication mode, serial data is transmitted and received on the RX pin. The TX pin is used as the transmit shift clock. Each frame transmits or receives 8 bits, with the low bit transmitted or received first
  - Mode 1: 10-bit full-duplex asynchronous communication, consisting of 1 start bit, 8 data bits, and 1 stop bit. The communication baud rate is variable
  - Mode 2: Reserved
  - Mode 3: 11-bit full-duplex asynchronous communication, consisting of 1 start bit, 8 data bits, 1 programmable 9th bit and 1 stop bit. The communication baud rate is variable
- Interrupts will be generated and corresponding flags TXIF and RXIF will be set when transmission and reception are complete. Interrupt flags need to be cleared by software
- UART0 and UART1 can generate DMA requests
- UART2 cannot generate DMA requests
- Independent baud rate generator
- UART2 does not support waking up from STOP Mode
- UART0/1 support waking up from STOP Mode:
  - The falling edge of the START bit can wake up STOP Mode
  - Provides corresponding wake-up interrupt enable bit WKIE and wake-up interrupt flag WKIF

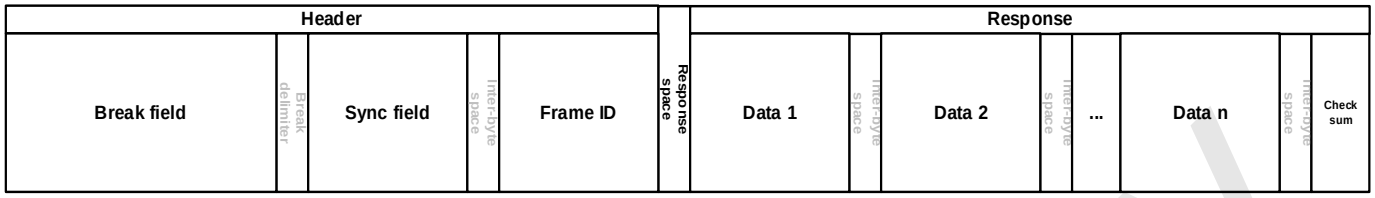
18.3 UART2-LIN

UART2 supports standard LIN communication protocol.

18.3.1 LIN Frame Structure

Under the LIN protocol, all communication information is encapsulated into frames. A frame is composed of a header (provided by the master task) and a response (provided by the slave task). The header (provided

by the master task) consists of a break field, a sync (synchronization) field and a frame ID. The frame ID serves solely to define the purpose of the frame and the slave is responsible for responding to the relevant frame ID. The response consists of a data field and a checksum field.



LIN Frame Structure Diagram

18.3.2 LIN Master Mode

By setting FUNCSEL=1 and SLVEN=0, the UART will support LIN master mode. In LIN mode, according to the LIN protocol, each byte is initiated with a dominant bit, followed by 8 data bits with no parity bit, LSB first, and ends with a recessive STOP bit.

The initialization process for LIN master mode is as follows:

① Configure the UART_BAUD register to set the baud rate.
② Set FUNCSEL=1 to select the LIN function mode.
③ Set SM[1:0] to 01 to configure the UART in Mode 1.

A complete header consists of a break field, a sync field, and a frame ID. The UART controller can choose the 'break field' as the transmitted header. The 'sync field' and 'frame ID field' need to be written by the user through software, that is to say, to send a complete header to the bus, the software must sequentially fill in the sync data (0x55) and the frame ID data into the UART_DAT register."

18.3.3 LIN Slave Mode

By setting FUNCSEL=1 and SLVEN=1, the UART will support LIN slave mode. In LIN mode, according to the LIN protocol, each byte is initiated with a dominant bit, followed by 8 data bits with no parity bit, LSB first, and ends with a recessive STOP bit.

The initialization process for LIN slave mode is as follows:

① Configure the UART_BAUD register to set the baud rate.
② Set FUNCSEL=1 to select the LIN function mode.
③ Set SM[1:0] to 01 to configure the UART in Mode 1.
④ Set SLVEN to 1 to enable LIN slave mod

In LIN slave mode, the slave break field detection function is enabled by setting LBDL to detect and receive 'break field'. After receiving a break, the BKIF flag will be set and an interrupt will be generated if BKIE is set to 1. To avoid bit rate deviation, users can set SLVAREN to enable automatic resynchronization feature to prevent clock errors.

18.3.4 Synchronization Error Detection

In automatic resynchronization mode, the controller will detect errors in the sync field. The error detection compares the current baud rate with the baud rate of the received sync field, and the following both detections are performed simultaneously.

Check 1: Based on the measurements from the first falling edge to the last falling edge of the sync field,

- If the error exceeds 15%, the header error flag SLVHEIF will be set.
- If the error is between 14% and 15%, the header error flag SLVHEIF may be set (depending on data dephasing).

Check 2: Based on the measurements from each falling edge of the sync field,

- If the error exceeds 19%, the header error flag SLVHEF will be set.
- If the error is between 15% and 19%, the header error flag SLVHEIF may be set (depending on data dephasing).

Note: Error detection is based on the current baud rate clock. Therefore, to ensure the accuracy of error detection, it is recommended that users reload the baud rate to its initial value through software before a new break field is received.

19 SPI0-1

19.1 Clock Source

The SC32F15G series SPI has only one clock source, which is derived from PCLK

19.2 SPI0 Feature

- Supports 11-stage SPI clock pre-scaling
- Signal ports can be mapped to another set of ports
- SPI0 signal ports strong driving
  - In SPI communication mode, the corresponding signal port's pin output driving capability will be enhanced, while in other modes, it remains consistent with the characteristics of a regular I/O.
  - Its mapped signal port can also be set to strong driving to ensure the consistency of SPI0 across any port
- Features a 16-bit 8-level FIFO with independent transmission and reception
  - SPI0's FIFO function allows continuous writing of 8 or fewer 16-bit transmit data to the SPI send buffer (SPI0_DATA). During SPI transmission, the data written into the FIFO first is also sent first. When the data written by the user to the FIFO is sent, the FIFO empty flag TXEIF will be set; if the FIFO is full, the write conflict flag WCOL will be set, and the user cannot write data to the FIFO until the data in the FIFO is sent out and the FIFO is not full. The interrupt flag SPIF will be set only when all the data in the FIFO has been sent
  - Continuously read 8 or fewer 16-bit receive data from the SPI receive buffer (SPI0_DATA), with the first received data being the first to be read
  - FIFO data transfer half-interrupt and corresponding flags for timely reading/writing of data:
    - Provides an interrupt and corresponding flag TXHIF when there is less than half of the valid data in the transmit FIFO
    - Provides an interrupt and corresponding flag RXHIF when there is more than half of the data in the receive FIFO
  - Support recieve buffer overflow interrupt and corresponding flag to promptly notify exceptions
- Support DMA
  - Enable TXDMAEN, and the DMA request can be triggered after the transmit buffer empty flag TXEIF is set, and TXEIF will be automatically cleared after DMA write transmit buffer.
  - Enable RXDMAEN, and the DMA request can be triggered after the receive buffer not empty status flag RXNEIF is set, and RXEIF will be automatically cleared after DMA read receive buffer.

19.3 SPI1 Feature

- SPI1 and TWI1 operate independently with multiplexed register addresses and signal pins
- Supports 13-stage SPI clock pre-scaling
- Signal ports can be mapped to three additional sets of ports
- No FIFO
- Supports DMA

19.4 SPI0 and SPI1 Comparison

Comparison / BIT	SPI0	SPI1
Signal Port Strong Driving	Available	None
WCOL	When the send FIFO is full, attempting to write to the FIFO will fail, and WCOL will be set, indicating a buffer write conflict	When one frame is sending, attempting to write to the FIFO will fail, and WCOL will be set, indicating a buffer write conflict
SPIF	This position being set indicates the completion of receiving/sending one frame of data	This position being set indicates the completion of receiving/sending one frame of data
QTWIF	None	This position being set indicates the completion of receiving/sending one frame of data
RXHIE	Interrupt enable bit for the valid data in the recieve FIFO is more than half	None
TXHIE	Interrupt enable bit for the valid data in the transmit FIFO is less than half	None
RXIE	Interrupt enable bit for the receive FIFO full	None
TBIE	Interrupt enable bit for the transmit FIFO empty	Interrupt enable bit for the transmit FIFO empty
RXNEIE	Interrupt enable bit for the receive FIFO not empty	None
RXHIF	Set when the valid data in the receive FIFO is more than half	None
TXHIF	Set when the valid data in the receive FIFO is less than half	None
RXFIF	Set when the receive FIFO is full	None
TXEIF	Set when the receive FIFO is empty	Set when the receive FIFO is empty
RXNEIF	Recieve FIFO not empty flag	None
DMA	Triggering DMA requests through the TXEIF flag and the RXNEIF flag	A request is uniformly set at the end of a frame

20 TWI0-1

20.1 Clock Source

The SC32F15G series TWI has only one clock source, which is derived from PCLK

20.2 TWI0 Feature

- Supports 11-stage TWI clock pre-scaling
- Signal ports can be mapped to two additional set of ports
- Support master/slave mode
- Bidirectional data transmission between master and slave
- Communication speed can reach up to 1 Mbps
- Support DMA

20.3 TWI1 Feature

- SPI1 and TWI1 operate independently with multiplexed register addresses and signal pins
- Supports 11-stage TWI clock pre-scaling
- Signal ports can be mapped to two additional set of ports
- Support master/slave mode
- Bidirectional data transmission between master and slave
- Communication speed can reach up to 1 Mbps

20.4 TWI Signal Description

On the TWI bus, data is synchronously transmitted between the master and slave devices using the clock line (SCL) and the data line (SDA). Each data byte has a length of 8 bits, and one data bit is transferred with each SCL clock pulse. The data is transmitted starting from the most significant bit (MSB), and after each byte, an acknowledgment bit follows. Each bit is sampled when SCL is high. Therefore, the SDA line may change when SCL is low, but it must remain stable when SCL is high. When SCL is high, any transition on the SDA line is considered a command (START or STOP)

TWI Clock Signal Line(SCL):

The clock signal is generated by the master and is connected to all the slaves. It transmits one byte of data every 9 clock cycles. The first 8 cycles are used for data transmission, and the last one is used as the acknowledgment clock for receiver. It should be pulled up by the pull-up resistor on the SDA line when idle.

TWI Data Signal Line(SDA)

SDA is a bidirectional signal line and should be pulled up by the pull-up resistor on the SDA line when idle.

21 Controller Area Network(CAN)

21.1 Overview

The Controller Area Network (CAN) in the SC32F15G series supports communication using both the CAN 2.0B protocol and the CAN FD protocol. Compared to the CAN 2.0B protocol, CAN FD offers greater flexibility, with a bit rate that can be adjusted (unlike the fixed 1 Mbit/s in CAN 2.0B) and a data field length of up to 64 bytes. The CAN module supports four different operating modes, including a low-power standby mode and wake-up functionality from standby.

The transmit buffer supports two types of transmission buffers: the PTB (Primary Transmission Buffer) and the STB (Secondary Transmission Buffer). The transmission order can be determined using either FIFO mode or priority mode. The receive buffer can store up to 8 frames simultaneously, and each received frame has an individual timestamp. Additionally, there are 8 configurable receive filters, each of which can be independently enabled and configured with specific filtering conditions.

21.2 Clock Source

The SC32F15G series CAN has only one clock source, which is derived from HCLK

21.3 Feature

- Protocol Support:
  - CAN 2.0B
    - Support standard format and extend format, maximum load 8 bytes data
    - Bit rate: 1Mbit/s
  - CAN FD
    - Support standard format and extend format, maximum load 64 bytes data
    - Variable bit rate: 1Mbit/s
- Supports low-power standby mode to reduce power consumption when the CAN interface is idle
- Time-Stamping:
  - CiA 603 Compliance, provides a 64-bit time-stamp for precise timing, each transmitted frame has one time-stamp stored in a register, and all received frames have individual time-stamps
- Transmit and Receive Buffers:
  - 8 Receive Buffers (RB)
  - 9 Transmit Buffers (TB)
    - 1 Primary Transmit Buffer(PTB)
    - 8 Secondary Transmit Buffer(STB), support FIFO mode or priority mode
  - 8 Receive Filters: Support 29-bit identifiers for filtering incoming messages

22 Hardware Watchdog WDT

The SC32F15G series features a built-in hardware watchdog (WDT) with an internal 32kHz oscillator as its clock source. Users can choose to enable the watchdog reset function by setting the ENWDT control bit in the Code Option through a programmer.

The hardware watchdog timer (WDT) is known for its high safety, accurate timing, and flexible usage. This watchdog peripheral can detect and resolve faults caused by software errors, and it will trigger a system reset when the counter reaches overflow time.

The WDT is driven by its internal low-frequency oscillator, which allows it to remain operational even if the main clock fails.

22.1 Clock Source

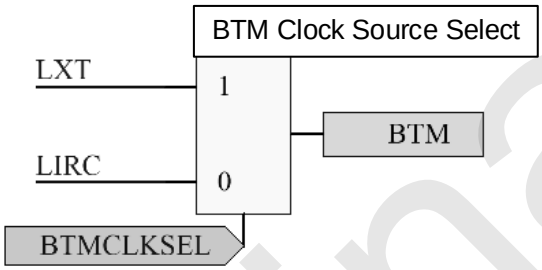
The SC32F15G series WDT is fixed to LIRC. Once the WDT is enabled, LIRC will automatically start, and it will remain oscillating throughout the operation of the WDT and users cannot turn off LIRC while the WDT is active.

23 Base Timer（BTM）

The SC32F15G series features a Base Timer (BTM) that can generate interrupts at intervals ranging from 15.625ms to 32s. The BTM can use either 32kHz LIRC or external 32.768kHz crystal oscillator (LXT) as its clock source. The interrupts generated by the BTM can wake up the CPU from STOP mode.

23.1 Clock Sourse

SC32F15G series BTM can choose LXT or LIRC as its clock sourse



23.2 Feature

- Selectable interrupt frequency intervals from 15.625ms to 32s
- Can wake up from STOP Mode

24 Built-in CRC Module

The SC32F15G series has a built-in CRC (Cyclic Redundancy Check) module that utilizes a polynomial generator to generate CRC codes from an 8-bit/16-bit/32-bit data word.

24.1 Clock Source

The SC32F15G series CRC has only one clock source, which is derived from HCLK.

24.2 Feature

- 1 built-in hardware CRC module
- Configurable initial value, with a default of 0xFFFF_FFFF
- Supports 8-bit/16-bit/32-bit data units
- Programmable polynomial, with a default of 0x04C1_1DB7
- Only supports software-driven data computation mode
- Supports DMA: CRC_DR can serve as the DMA destination address or be accessed directly via registers
- Calculating CRC for a single byte requires 1 system clock

CRC algorithm	CRC-32/MPEG-2
Polynomial Formula	$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^{8}+x^{7}+x^{5}+x^{4}+x^{2}+x+1$
Data Width	32bit
Inital Value	0xFFFF_FFFF
Result XOR Value	0x0000_0000
Input Value Reversal	false
Output Value Reversal	false
LSB/MSB	MSB

Note: The written and read data in CRCDR cannot be the same.

25 Direct Memory Access (DMA)

25.1 Overview

The DMA controller is designed for high-speed data transfer, allowing the movement of data from one address to another without the need for CPU intervention. Leveraging DMA for data transfer can reduce the workload on the CPU, enabling the saved CPU resources to be utilized for other applications. The DMA controller comprises 4 channels, each directly connected to dedicated hardware DMA requests. Additionally, each channel supports software triggering. The DMA controller features support for 4-level channel priority, facilitating the management of priority between DMA requests to ensure that only one DMA channel operates at any given time. It also supports both single and batch transfers, with the request source being either a software request or an interface request. Data transfer between memories is accomplished using software requests.

Note: For a bidirectional data transfer application, two DMA channels are required to handle sending and receiving operations.

25.2 Clock Source

The clock source of DMA is derived from HCLK, and the external peripheral clock of DMA is enabled through AHB_CFG.DMAEN.

25.3 Feature

- Support 4 independent configurable channels
- Support 4 priority levels for requests
- Support 8-bit, 16-bit, 32-bit data transfers
- Support automatic increment or fixed source and destination addresses, with data widths of byte, half-word, and word
- Support single and burst transfer modes

25.4 Function Description

25.4.1 Transmission

No transmit limitation between peripheral and memory for DMA：

Memory-to-Memory	Memory-to-Peripheral	Peripheral-to-Memory	Peripheral-to-Periphral
No limitation	No limitation	No limitation	No limitation

25.4.2 DMA Access Restriction

Users are not allowed to perform write operations on Flash or access the core through DMA. Violating these restrictions may lead to unpredictable exceptions.

25.4.3 Channel Priority

There are 4 priority levels can be configured through PL[1:0] registers:

- 00: Low
- 01: Medium
- 10: High
- 11: Very High

25.4.4 Single Transmission and Burst Transmission

The DMA controller supports single and burst data transfer types, and the request source can be a software request or an interface request while data transfer between memory is done by software requests. Single transfer means that the software or interface is ready to transfer one data (each data requires one request), while burst transfer means that the software or interface will transfer multiple data (multiple data requiring only one request).

The modes of single and burst transfer can be set through TPTYPE register (DMAn_CFG[15]).

In single transfer mode, each transfer of data requires one request. As each data is transferred, the values in the register DMAn_CNT[31:0](n=0-3) decrease by 1, the transfer of data is completed when the count in DMAn_CNT[31:0] becomes 0. In this mode, BURSIZE (DMAn_CFG[14:12]) is not used to control the size of the transferred data and its value is fixed at 1.

In burst transfer mode, DMA transfer DMAn_CNT[31:0] data with only one request. After transferring BURSIZE (DMAn_CFG[14:12]) data, the value in DMAn_CNT[31:0] is decreased by BURSIZE. The transfer of data is completed when the count in DMAn_CNT[31:0] becomes 0.

25.4.5 Loop Mode

The loop mode can be used to handle circular buffers and continuous data streams (such as ADC scan mode). During the loop mode transfer, the number of data to be transferred will automatically reload to the initial value set in the channel configuration phase and continue to respond to DMA requests. To stop loop transfer, the software needs to stop the generation of DMA requests by the peripheral before disabling the DMA channel (for example, exiting ADC scan mode). The software must explicitly set the DMACNT value before starting/enabling the transfer and after stopping the loop transfer.

The SC32F15G series DMA controller supports normal mode and loop mode:

- When CIRC=0 (DMA channel is in non-loop mode), it will no longer accept any DMA requests after reaching the set number of data to be transferred
- When CIRC=1 (DMA channel is in loop mode), after the transfer is complete, the DMACNT of the channel will automatically reload the previously set value and wait for the next loop

Users can flexibly choose according to their actual needs.

25.4.6 DMA Channel Control Bit Restrictions After Enable

Once a DMA channel is enabled (CHEN = 1), certain control bits become read-only to prevent modifications during an active DMA transfer, which could lead to unpredictable data transmission behavior.

After DMA channel is enabled, register bit fields/bits, source and destination addresses, priority settings and transfer control configurations are locked.

26 SysTick

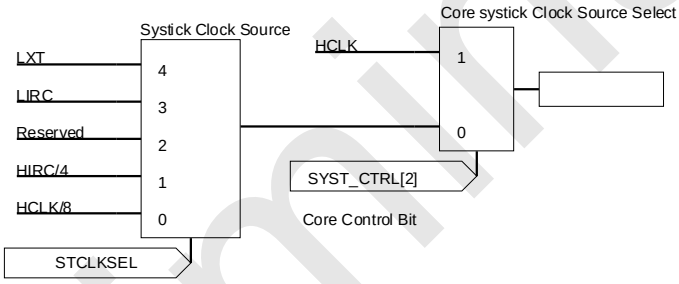
SysTick is a simple, 24-bit, writable-clear, decrementing automatic reload counter with a flexible control mechanism. This counter can be used as a tick timer for a Real-Time Operating System (RTOS) or as a simple counter.

26.1 Clock Source

SysTick (Cortex®-M0+ Core System Timer) has internal clock source and external clock source：

- Internal clock source: CPU Clock
- 4 external clock sources

SysTick clock sourse diagram is as follow:



26.2 SysTick Calibration Register Default Value

The calibration value for the SysTick Calibration Register is set as follows:

- If the default clock after power-on is f_{HCLK}/n (MHz), where n is the default power-on divider, and the default clock source is HIRC
- Then, setting the initial SysTick calibration value to 1000 * (f_{HCLK}/n) will generate a 1ms time reference

27 Electrical Characteristics

Unless otherwise specified, the electrical data in this section are based on the working conditions listed in the “Recommended Operating Conditions” subsection.

27.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	DC supply voltage	-0.3	6	V
V_{PIN}	Input/output voltage of any pin	-0.3	V_{DD}+0.3	V
T_A	Ambient temperature	-40	105	℃
T_{STG}	Storage temperature	-55	125	℃
I_{VDD}	Current value flowing through VDD	-	200	mA
I_{VSS}	Current value flowing through VSS	-	200	mA

27.2 Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit	Conditions
V_{DD}	Operating voltage	2.0	5.5	V	f_{HCLK}=72MHz Clock source is HIRC
T_A	Ambient temperature	-40	105	℃	

Symbol	Parameter	Min	Max	Unit	Conditions
f_{HCLK}	Internal AHB clock frequency	-	72	MHz	T_A = +25℃
f_{PCLK}	Internal APB clock frequency	-	72	MHz	

27.3 Flash ROM Parameters

VDD = 5V,TA = +25℃,unless otherwise specified

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
N_{END}	Endurance earse/write cycles	100,000	-	-	Cycles	Clock source is HIRC
T_{DR}	Data retention time	100	-	-	Years	
$T_{S\text{-}Erase}$	Single sector erase time	-	2.5	-	ms	
T_{Erase}	Page erase time	30	-	40	ms	
T_{Write}	Single byte write time	-	150	-	μs	

27.4 Power Consumption

27.4.1 VDD = 5V,TA = +25℃,unless otherwise specified

Symbol	Parameter	Boot Area	Min	Typical	Max	Unit	Conditions
I_{op1}	Operating current	APROM	-	7	-	mA	f_{HCLK}=72MHz Clock source is HIRC
			-	4	-	mA	f_{HCLK} =36MHz Clock source is HIRC
			-	2.9	-	mA	f_{HCLK} =18MHz Clock source is HIRC
			-	2.3	-	mA	f_{HCLK} =9MHz Clock source is HIRC
			-	1.7	-	mA	f_{HCLK} =4.5MHz Clock source is HIRC
I_{pd1}	Power Down Mode current	APROM	-	2.3	-	μA	
I_{IDL1}	IDLE Mode current	APROM	-	2.8	-	mA	f_{HCLK} =72MHz Clock source is HIRC

27.4.2 VDD = 3.3V,TA = +25℃,unless otherwise specified

Symbol	Parameter	Boot Area	Min	Typical	Max	Unit	Conditions
I_{op2}	Operating current	APROM	-	7	-	mA	f_{HCLK}=72MHz Clock source is HIRC
			-	4	-	mA	f_{HCLK} =36MHz Clock source is HIRC
			-	2.9	-	mA	f_{HCLK} =18MHz Clock source is HIRC
			-	2.3	-	mA	f_{HCLK} =9MHz Clock source is HIRC
			-	1.7	-	mA	f_{HCLK} =4.5MHz Clock source is HIRC
I_{pd2}	Power down Mode current	APROM	-	2.2	-	μA	
I_{IDL2}	IDLE Mode current	APROM	-	2.8	-	mA	f_{HCLK} =72MHz Clock source is HIRC

27.5 GPIO Parameter

27.5.1 VDD = 5V,TA = +25℃,unless otherwise specified

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
V_{IH1}	Input high voltage	$0.7V_{DD}$	-	V_{DD}+0.3	V	
V_{IL1}	Input low voltage	-0.3	-	$0.3V_{DD}$	V	
V_{IH2}	Schmitt trigger input high voltage	$0.8V_{DD}$	-	V_{DD}	V	Schmitt trigger input: NRST T_CLK / T_DIO UART0 enter RX SPI / TWI signal input INT0-INT15 PWM fault detection port FLT Timer clock input Tn Timer capture port TnEX
V_{IL2}	Schmitt trigger input low voltage	-0.2	-	$0.2V_{DD}$	V	
I_{OL1}	Regular driving IO ports Output low current	-	30	-	mA	V_{Pin}=0.4V
I_{OL2}	Regular driving IO ports Output low current	-	54	-	mA	V_{Pin}=0.8V
I_{OH1}	Output high current @ V_{Pin}=4.3V	-	12	-	mA	Pxyz=0,I_{OH} level 0
		-	9	-	mA	Pxyz=1,I_{OH} level 1
		-	6	-	mA	Pxyz=2,I_{OH} level 2
		-	3.2	-	mA	Pxyz=3,I_{OH} level 3
I_{OH2}	Output high current @ V_{Pin}=4.7V	-	6	-	mA	Pxyz=0,I_{OH} level 0
		-	4	-	mA	Pxyz=1,I_{OH} level 1
		-	3.1	-	mA	Pxyz=2,I_{OH} level 2
		-	1.6	-	mA	Pxyz=3,I_{OH} level 3
I_{lkg1}	Input leakage current	-1	-	1	μA	IO is in high-impedance input mode V_{IN}=V_{DD} or V_{SS}
R_{PH1}	Pull-up resistance	15	30	45	kΩ	V_{IN}=V_{SS}

27.5.2 VDD = 3.3V,TA = +25℃, unless otherwise specified

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
V_{IH3}	Input high voltage	$0.7V_{DD}$	-	V_{DD}+0.3	V	

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
V_{IL3}	Input low voltage	-0.3	-	$0.3V_{DD}$	V	
V_{IH4}	Input high voltage	$0.8V_{DD}$	-	V_{DD}	V	Schmitt trigger input: NRST T_CLK / T_DIO UART0 enter RX SPI / TWI signal input INT0-INT15 PWM fault detection port FLT Timer clock input Tn Timer capture port TnEX
V_{IL4}	Input low voltage	-0.2	-	$0.2V_{DD}$	V	
I_{OL3}	Regular driving IO ports Output low current	-	22	-	mA	V_{Pin}=0.4V
I_{OL4}	Regular driving IO ports Output low current	-	37	-	mA	V_{Pin}=0.8V
I_{OH3}	Output high current @ V_{Pin}=3.0V	-	3.8	-	mA	Pxyz=0,I_{OH} level 0
		-	3.0	-	mA	Pxyz=1,I_{OH} level 1
		-	2.0	-	mA	Pxyz=2,I_{OH} level 2
		-	1.0	-	mA	Pxyz=3,I_{OH} level 3
I_{lkg2}	Input leakage current	-1	-	1	μA	IO is in high-impedance input mode V_{IN}=V_{DD} or V_{SS}
R_{PH2}	Pull-up resistance	25	50	75	kΩ	V_{IN}=V_{SS}

27.6 BTM Characteristics

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
I_{BTM}	Base Timer working current @5V	-	1.1	3	μA	Clock source is LIRC
	Base Timer working current @3.3V	-	1.1	3	μA	Clock source is LIRC

27.7 WDT Characteristics

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
I_{WDT}	WDT working current @5V	-	1.1	3	μA	Clock source is LIRC
	WDT working current @3.3V	-	1.1	3	μA	Clock source is LIRC

27.8 AC Electrical Characteristics

(V_{DD} = 2.0V - 5.5V,T_A = 25℃,unless otherwise specified)

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
T_{LXT}	External 32kHz oscillator start-up time	-	1	-	s	External 32kHz crystal oscillator
T_{POR}	Power On Reset time	-	15	-	ms	
T_{PDW}	Power Down Mode wake-up time	-	65	130	μs	
T_{Reset}	Reset pulse width	18	-	-	μs	low-level active
T_{LVR}	LVR debounce time	-	30	-	μs	
f_{HIRC}	HIRC oscillator stability	71.28	72	72.72	MHz	V_{DD}=2.0-5.5V T_A=-40 to 105 ℃
f_{LIRC}	LIRC oscillator stability	30.72	32	33.28	kHz	V_{DD}=4.0-5.5V T_A=-20 to 85 ℃

27.9 ADC Characteristics

(T_A = 25℃,unless otherwise specified)

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
V_{ADC}	Supply Voltage	2.0	5.0	5.5	V	Vref = 1.024V
		2.7	5.0	5.5	V	Vref = 2.048V
		2.7	5.0	5.5	V	Vref = 2.4V
		2.0	5.0	5.5	V	Vref = V_{DD}
N_R	Precision	-	12	-	bit	GND≤V_{AIN}≤V_{DD}
V_{AIN}	ADC Input voltage	GND	-	V_{DD}	V	
R_{AIN}	ADC Input resistance	1	-	-	MΩ	V_{IN}=5V
C_{ADC}	ADC Internal sampling capacitance	-	8	-	pF	
I_{lkg_ADC}	Input leakage current	-1	-	1	μA	V_{IN}=V_{DD} or V_{SS}
I_{ADC}	ADC conversoin current	-	2.5	3	mA	ADC Module on V_{DD}=5V
		-	2.0	2.5	mA	ADC Module on V_{DD}=3.3V
DNL	Differential nonlinear error	-	±3	-	LSB	V_{DD}=5V V_{REF}=5V
INL	Integral nonlinear error	-	±3	-	LSB	
SNR	Signal-noise ratio	-	65.4	-	dB	
THD	Total harmonic distortion	-	-70.5	-	dB	

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
SINAD	Signal-to-noise-and-distortion ratio	-	64.3	-	dB	
SFDR	Spurious free dynamic range	-	73.0	-	dB	
ENOB	Effective-number-of-bits	-	10.5	-	bits	
E_Z	Offset error	-	±2	-	LSB	
E_F	Full scale error	-	±3	-	LSB	
E_{AD}	Total absolute error	-	±3	-	LSB	
T_{ADCT}	ADC conversion time	-	404	-	ns	f_{HCLK} =72MHz，Clock source is HIRC
T_{ADCS}	ADC sampling time	-	0.06	-	μs	LOWSP[2:0] = 000 f_{HCLK} =72MHz，Clock source is HIRC
			0.09	-	μs	LOWSP[2:0] = 001 f_{HCLK} =72MHz，Clock source is HIRC
			0.14	-	μs	LOWSP[2:0] = 010 f_{HCLK} =72MHz，Clock source is HIRC
			0.23	-	μs	LOWSP[2:0] = 011 f_{HCLK} =72MHz，Clock source is HIRC
			0.43	-	μs	LOWSP[2:0] = 100 f_{HCLK} =72MHz，Clock source is HIRC
		-	0.85	-	μs	LOWSP[2:0] = 101 f_{HCLK} =72MHz，Clock source is HIRC
		-	1.69	-	μs	LOWSP[2:0] = 110 f_{HCLK} =72MHz，Clock source is HIRC
		-	6.67	-	μs	LOWSP[2:0] = 111 f_{HCLK} =72MHz，Clock source is HIRC

27.10 CMP Electrical Characteristics

(V_{DD} =5V,T_A = 25℃, unless otherwise specified)

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
V_{CM}	Input voltage range	0	-	V_{DD}	V	
V_{OS}	Offset voltage	-	2	6	mV	

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
V_{HYS}	Comparator voltage hysteresis	-	0	-	mV	HYS=00
		-	5	-	mV	HYS=01
		-	10	-	mV	HYS=10
		-	20	-	mV	HYS=11
I_{CMP0-2}	Comparator 0-2 switching current	-	75	-	μA	V_{DD}=5V
I_{CMP3}	Comparator 3 switching current	-	100	-	μA	
T_{CMP}	Response time	-	50	-	ns	

27.11 OP Electrical Characteristic

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
I_{OP}	OP working current	-	1	1.3	mA	V_{DD}=5V
V_{OP}	OP working voltage	2.8	-	5.5	V	
V_{OPO}	OP output voltage	V_{SS}+0.2	-	V_{DD}-0.2	V	
V_{CMI}	Common mode input voltage	0	-	V_{DD}	V	
V_{OFFSET}	Offset voltage	-1	-	1	mV	
I_{LOAD}	Load current	-	-	600	μA	
R_{LOAD}	Load resistance	8	-	-	kΩ	
C_{LOAD}	Load capacitance	-	-	30	pF	
CMRR	Common mode rejection ratio	-	90	-	dB	
PSRR	Power supply rejection ratio	-	75	-	dB	
GBW	Gain-bandwidth	-	40	-	MHz	
Slew rate	Slew rate	-	13	-	V/us	
PM	Phase margin	-	60	-	°	CL = 50pF
G_{PGA}	PGA non-inverting gain	-5	-	5	%	Non-inverting gain = 4
		-5	-	5	%	Non-inverting gain = 8
		-5	-	5	%	Non-inverting gain = 16
		-5	-	5	%	Non-inverting gain = 32
	PGA inverting gain	-5	-	5	%	Inverting gain = 3
		-5	-	5	%	Inverting gain = 7
		-5	-	5	%	Inverting gain = 15

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
		-5	-	5	%	Inverting gain = 31
R_{PGA}	PGA non-inverting R2/R1 internal resistance value	-	30/10	-	kΩ/ kΩ	Non-inverting gain = 4
		-	70/10	-	kΩ/ kΩ	Non-inverting gain = 8
		-	150/10	-	kΩ/ kΩ	Non-inverting gain = 16
		-	310/10	-	kΩ/ kΩ	Non-inverting gain = 32
	PGA inverting R2/R1 internal resistance value	-	30/10	-	kΩ/ kΩ	Inverting gain = 3
		-	70/10	-	kΩ/ kΩ	Inverting gain = 7
		-	150/10	-	kΩ/ kΩ	Inverting gain = 15
		-	310/10	-	kΩ/ kΩ	Inverting gain = 31
RΔ	R1/R2 resistance variation	-20	-	+20	%	

Note: Offset voltage(V_{OFFSET}) and phase margin(PM) are guaranteed by design

27.12 DAC Electrical Characteristic

(V_{DD} =5V,T_A = 25℃, unless otherwise specified)

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
V_{DAC}	Supply Voltage	2.0	5.0	5.5	V	Vref = 1.024V
		2.7	5.0	5.5	V	Vref = 2.048V
		2.7	5.0	5.5	V	Vref = 2.4V
		2.0	5.0	5.5	V	Vref = V_{DD}
N_R	Precision	-	10	-	bit	
V_{AIN}	DAC Output voltage	GND	-	V_{DD}-0.2	V	
R_{AIN}	DAC load resistance	5	-	-	kΩ	
F_{AIN}	DAC load capacitance	-	-	50	pF	
I_{DAC1}	DAC working current 1 Full-Scale output		0.27	-	mA	Full-Scale Output
I_{DAC2}	DAC working current 2 Zero output		0.26	-	mA	Zero Output
DNL	Differential nonlinear error (VDD=5V,V_{REF}=5V)		±1		LSB	
INL	Integral nonlinear error (VDD=5V,V_{REF}=5V)		±2		LSB	
OFFSET	Offset voltage	-	±20		mV	
T_{DAC1}	DAC conversion time 1 0->5V	-	1	-	μs	

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
T_{DAC2}	DAC conversion time 2 5V->0	-	1	-	μs	
T_{DAC3}	DAC conversion time 3 0->2.5V	-	0.5	-	μs	
T_{DAC4}	DAC conversion time 4 2.5V->0	-	0.5	-	μs	

27.13 VREF Electrical Characteristic

(V_{DD} =5V,T_A = 25℃, unless otherwise specified)

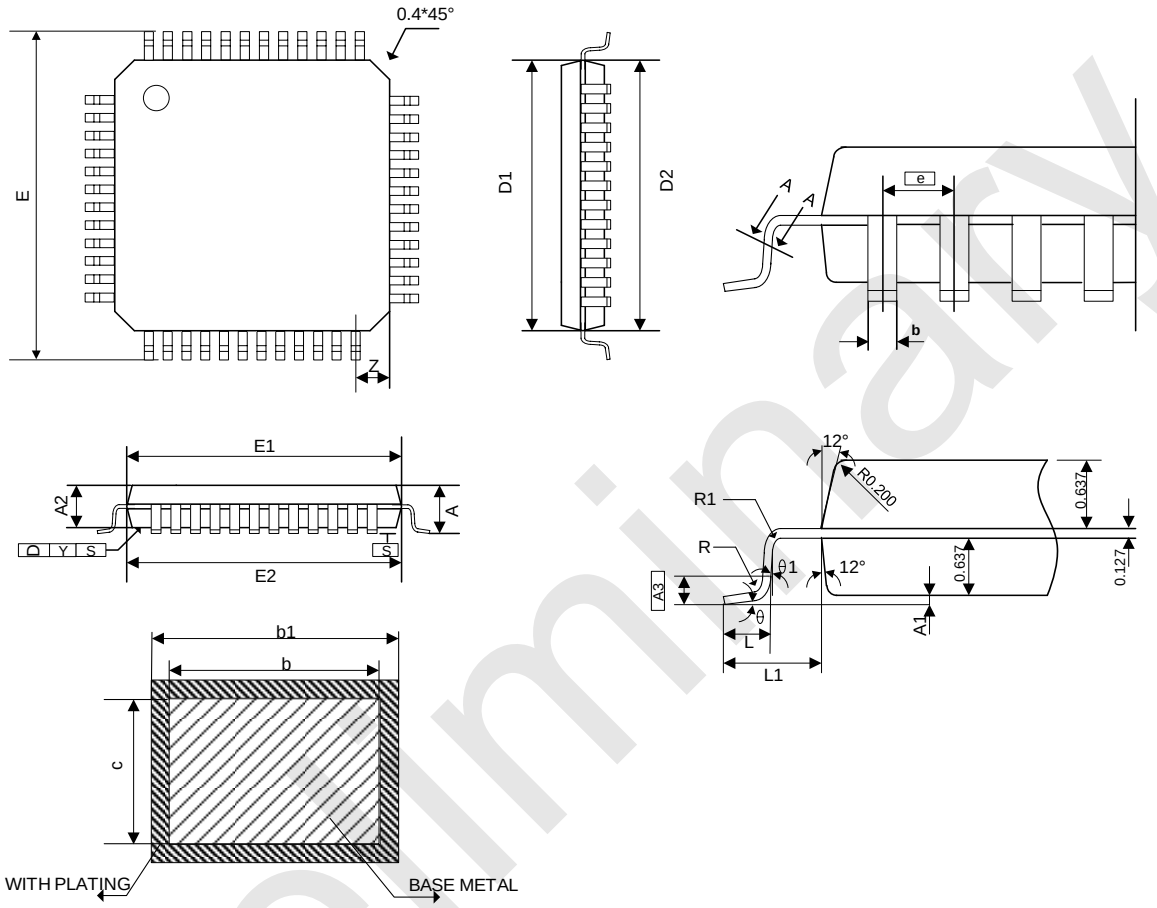
Symbol	Parameter	Min	Typical	Max	Uint	Conditions
V_{REF1}	Internal reference 2.048V	2.028	2.048	2.068	V	V_{DD} = 2.7 to 5.5V
V_{REF2}	Internal reference 1.024V	1.004	1.024	1.044	V	V_{DD} = 2.0 to 5.5V
V_{REF3}	Internal reference 2.4V	2.38	2.40	2.42	V	V_{DD} = 2.7 to 5.5V

27.14 Temperature Sensor Electrical Characteristic

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
α_{TS}	Voltage temperature coefficient	-	5	-	mV/℃	V_{ref}=2.4V
V_{25}	Voltage under 25℃	-	1.48	-	V	
T_{STRAT}	Setup time	-	10	-	μs	
T_{S_temp}	Sampling time when ADC channel select temperature sensor	-	2	-	μs	

28 Package information

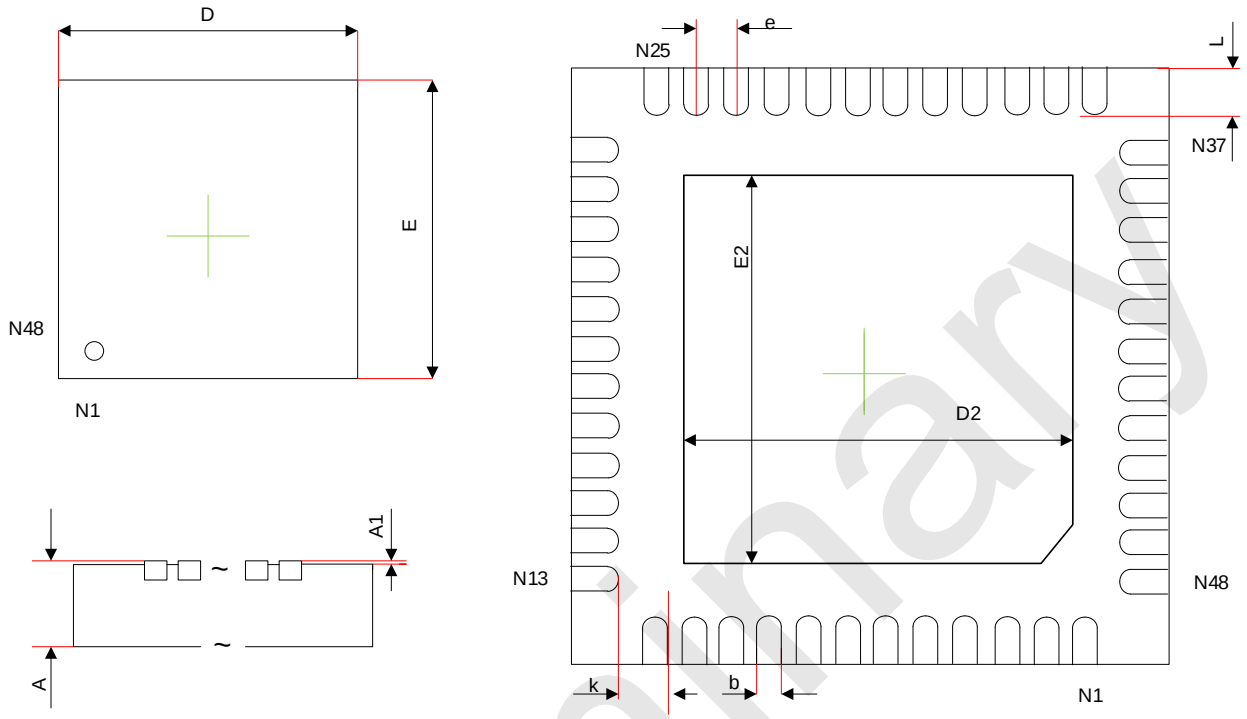
LQFP48 (7X7) Dimension (Unit: mm)



Symbol	mm(milimetre)		
	Min	Normal	Max
A	1.45	1.55	1.65
A1	0.01	--	0.21
A2	1.3	1.4	1.5
A3	--	0.254	--
b	0.15	0.20	0.25
b1	0.16	0.22	0.28
c	0.12	--	0.17
D1	6.85	6.95	7.05
D2	6.90	7.00	7.10
E	8.8	9.00	9.20

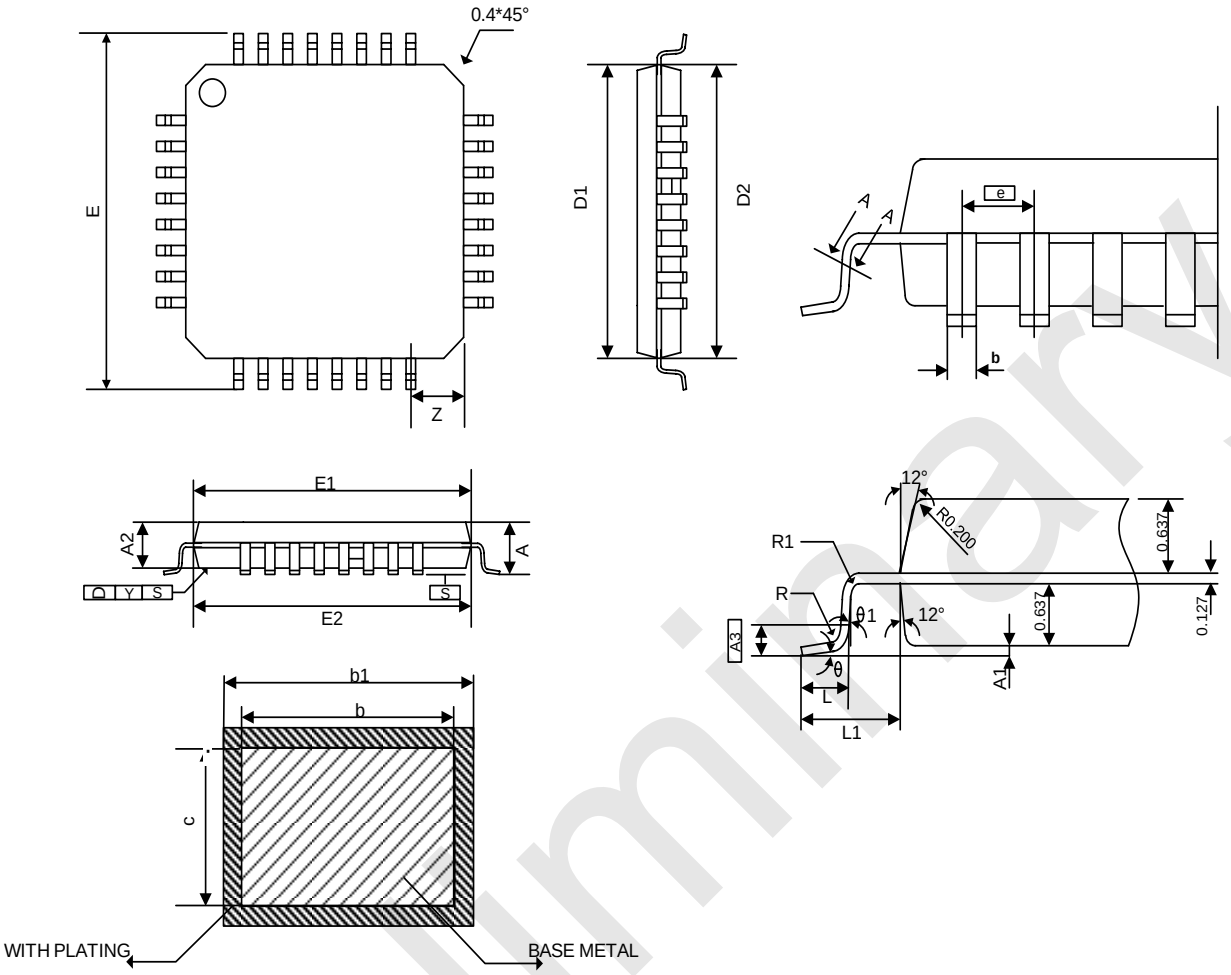
Symbol	mm(milimetre)		
	Min	Normal	Max
E1	6.85	6.95	7.05
E2	6.9	7.00	7.10
e	--	0.5	--
L	0.43	--	0.75
L1	0.90	1.0	1.10
R	0.1	--	0.25
R1	0.1	--	--
θ	0°	--	10°
θ1	0°	--	--
y	--	--	0.1
Z	--	0.75	--

QFN48 (5X5) Dimension (Unit: mm)



Symbol	mm(milimetre)		
	Min	Normal	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.12	--	0.23
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
e	0.35 BSC.		
k	0.20	0.30	--
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
L	0.30	0.35	0.40

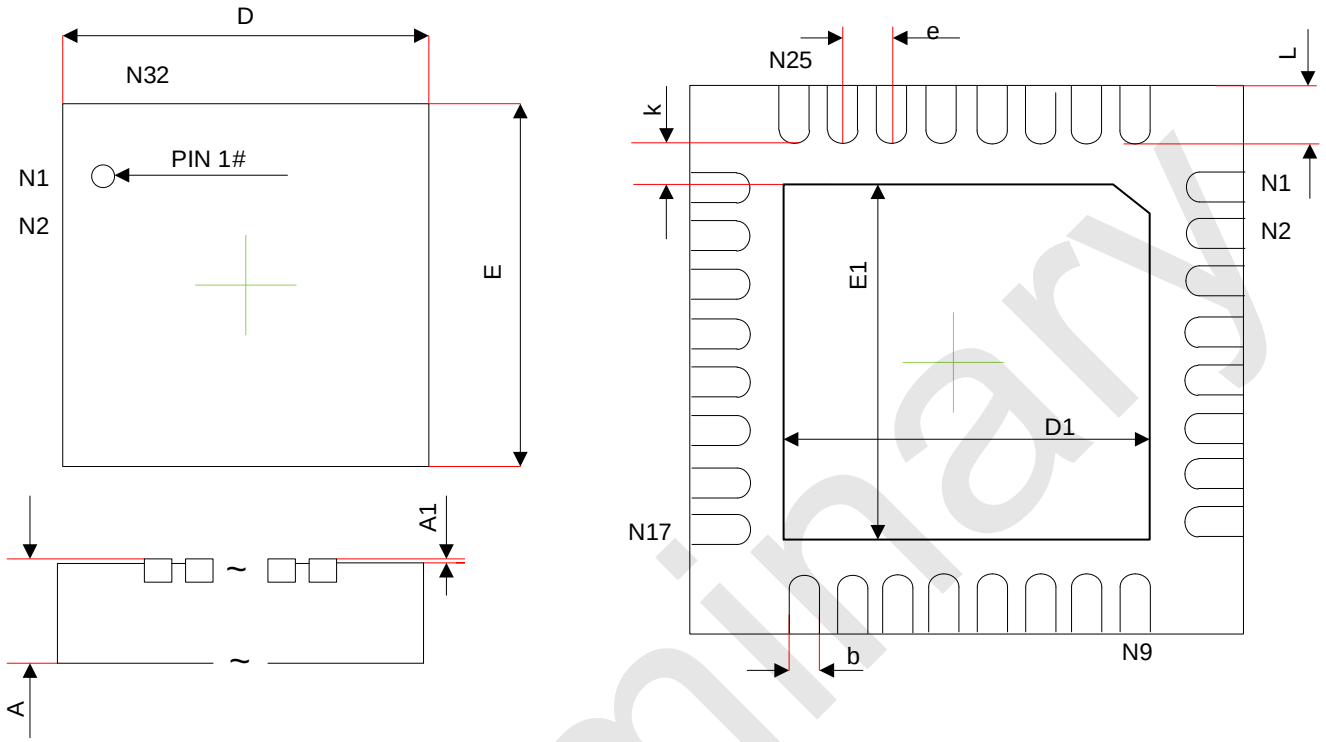
LQFP32 (7X7) Dimension (Unit: mm)



Symbol	mm(milimetre)		
	Min	Normal	Max
A	1.45	1.55	1.65
A1	0.01	--	0.21
A2	1.30	1.4	1.5
A3	--	0.254	--
b	0.30	0.35	0.41
b1	0.31	0.37	0.43
c	0.12	0.13	0.14
D1	6.85	6.95	7.05
D2	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.85	6.95	7.05
E2	6.90	7.00	7.10

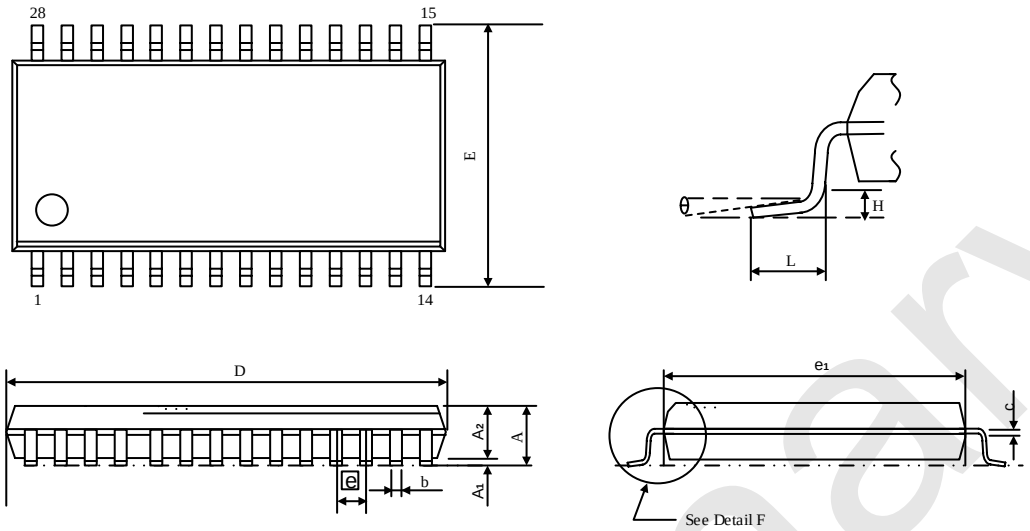
Symbol	mm(milimetre)		
	Min	Normal	Max
e	--	0.8	--
L	0.43	--	0.75
L1	0.90	1.0	1.10
R	0.1	--	0.25
R1	0.1	--	--
θ	0°	--	10°
θ1	0°	--	--
y	--	--	0.1
Z	--	0.70	--

QFN32 (4X4) Dimension (Unit: mm)



Symbol	mm(milimetre)		
	Min	Normal	Max
A	0.70	0.75	0.80
A1	--	0.02	0.05
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e	0.40 BSC		
k	0.2	--	--
D1	2.60	--	2.90
E1	2.60	--	2.90
L	0.22	--	0.45

TSSOP28L Dimension (Unit: mm)



Symbol	mm(milimetre)		
	Min	Normal	Max
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	9.600	-	9.800
E	6.250	-	6.550
e1	4.300	-	4.500
e	0.65(BSC)		
L	-	-	1.0
θ	0°	-	8°
H	0.05	-	0.25

29 Revision History

Version	Notes	Date
V0.1	Initial Release	2025.02.10

30 Important Notice

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